

**Evaluation of Potential Applications for Templated Arrays of
Heterostructural Semiconductor Nanowires as Light Emitting Devices**

by

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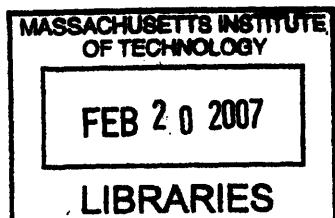
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ABSTRACT

While light emitting devices, such as laser diodes (LDs) and light emitting diodes (LEDs), were first introduced decades ago, they have been the subject of continuing research and improvements due to their relatively poor performance. Evolution has occurred in both the design of light emitting devices and in the materials from which they are made. This thesis examines new proposals for use of templated arrays of heterostructural semiconductor nanowire light emitting devices, from both engineering and business points of view. The effects of wire spacing and diameter on reliability and performance (both the internal quantum efficiency and the extraction efficiency) are evaluated. Business models for development of nanowire arrays for light emitting devices are discussed.

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Chapter 1 Introduction

Professor Charles M. Lieber from Harvard, the co-founder of Nanosys, once said in 2003:

“It will be essential to learn more about the basic physics of the nanowire lasers before they are used in real-world devices, but some simple applications could be ready in less than five years.”

Research groups all over the world have been working on light emitting devices, especially laser diodes (LDs) and light emitting diodes (LEDs), for decades, with a focus on improving the properties of optoelectronic devices. Since the light-emitting mechanisms are well understood, finding new device structures or alternative materials has been the main direction of research. Nanowire arrays stand out as useful candidates, due to their extraordinary optoelectronic properties and much simpler self-assembly fabrication method.

This thesis analyzes the advantages of the templated arrays of heterostructural semiconductor nanowires and evaluates their application for formation of light emitting devices.

First, in Chapter 2, the basic structure design of the device and the fundamental theory of

light emission in heterojunctional semiconductor nanowire structures are reviewed. Then, several alternative technologies for fabrication of the arrayed structure are briefly discussed. The main bodies of chapters 3 and 4 will give a full analysis of how nanowire-array LEDs compete with other light emitting devices, and an examination of the trade-off between the enhanced reliability of the structure and the possibly degraded performance of the devices. Chapter 5 reports an investigation of the associated intellectual property for nanowire-array LEDs. Finally, the potential market and business models are discussed, and a short-term solution for a start-up company will be suggested.

Chapter 2 Background Theory and Technology

2.1. Fundamentals of LED and LD

2.1.1. Light Emitting Mechanism in LEDs and LDs

The radiative recombination of electron-hole pairs (EHPs) applied in commercialized light emitting devices leads to the generation of electromagnetic radiation--- light emission--- by electric current injection in a p-n junction, usually fabricated from a direct band gap material such as GaAs or GaN. Such a device based on the spontaneous emission is called a light emitting diode, LED. If mirrors are provided to make a resonant cavity and the concentration of the EHPs (called the injection level) exceeds certain critical value to fulfill the requirement of *population inversion* for stimulated emission, this device can then function as a semiconductor laser diode, LD, that emits coherent light with all the photons in phase with each other.

Nowadays, high-power LEDs normally make use of multiple 2-dimensional Quantum Wells (QW) for the active region to get a much higher radiative recombination (internal quantum efficiency) compared to old low-power LEDs, while, LDs add the Separate Confinement Heterostructure (SCH) of the cladding layers with a larger/wider energy bandgap and a lower refractive index above and below the active region, to take advantage of both Double Heterostructure (DH) and QW effects, achieving high

confinement of not only current (electrons), coupled with the modulation doping technology, but also light (photons) without a large applied field. The structure of a typical GaAs laser is schematically shown below. For comparison, an LED structure is very similar, but without the resonant cavity or the controlled emitting region to create conditions for stimulated emission by either designing the shape and size of the active region, or selectively positioning the metal contact and/or adding the current blocking barrier.

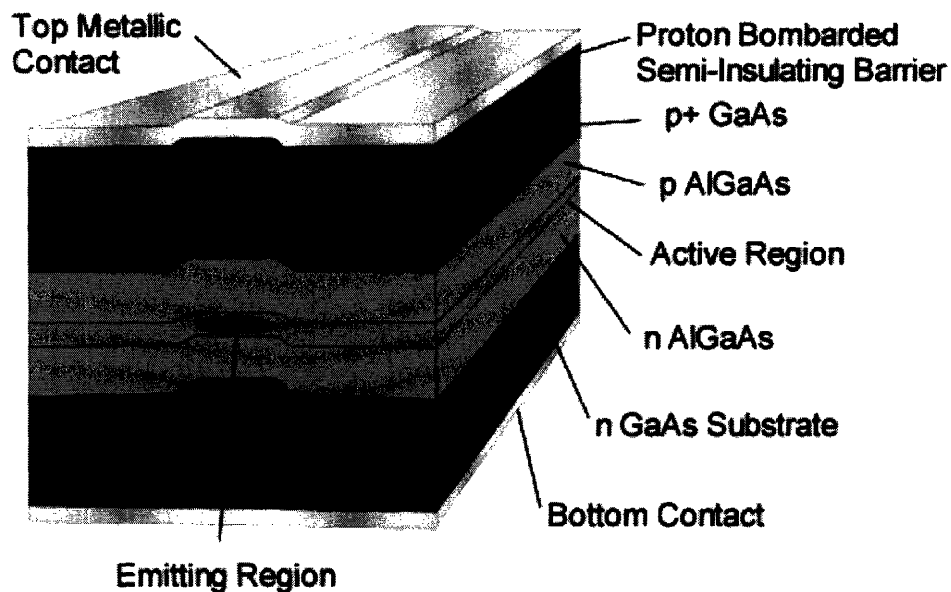


Figure 1¹: Schematic diagram of a typical GaAs edge-emitting laser.

There are two classes of lasers: edge-emitting lasers and vertical cavity surface-emitting lasers (VCSELs). The differences lay in the formation of the resonant cavity. The former has the mirrors on the front and back sides of the structure (created by the cleavage of the crystallographic surfaces), while the latter is fabricated by growing

Distributed Bragg Reflector (DBR) layers on top and bottom of the active region to function as the mirrors, as sketched in Figure 2.

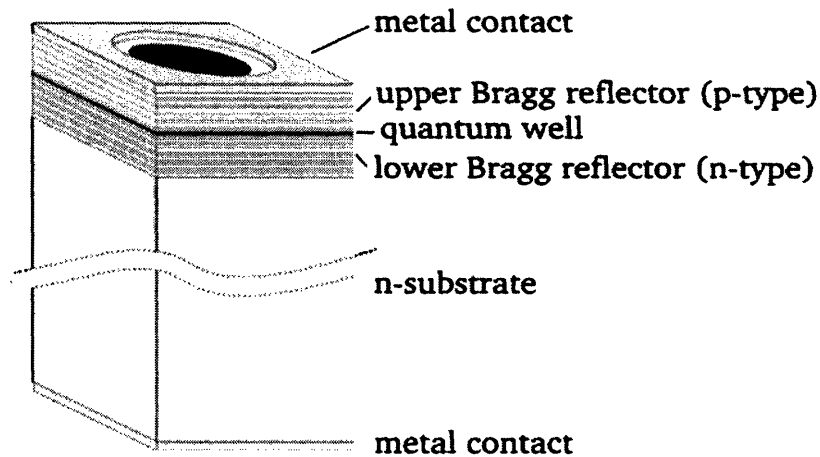


Figure 2²: Schematic diagram of simple VCSEL structure.

Operation of an LD is characterized by a threshold current. Figure 3 shows the output characteristics of an LD as a function of the input current. At low values of the input current, the device acts like an LED, producing a relatively small amount of incoherent light with random phases and directions. At the threshold value, where the population inversion is large enough so that the optical gain can overcome the losses, the transition from spontaneous emission to the stimulated emission takes place. As current increases above the lasing-threshold value, the light output increases much more rapidly with the emission peak of a much narrower wavelength range than in the LED region. The light is now the coherent laser light.

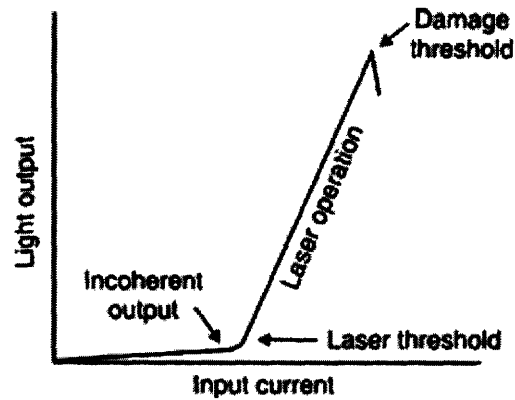


Figure 3³: Schematic diagram of the output of a laser diode as a function of the drive current.

Since an LD can be treated as a natural, but a bit more complicated progression from an LED, the performance examination in Chapter 4 will focus more on the LED application.

2.1.2. Drawbacks of Current Light Emitting Devices

Current light-emitting devices are suffering many limitations, such as poor extraction efficiency of light (low external quantum efficiency), high threading dislocation (TD) density, structure damages and so on.

To further explain:

Poor extraction efficiency occurs when photons generated by EHPs cannot be transported out of the device, but are reabsorbed by the material itself. Dislocations are formed by lattice mismatches and/or differences of coefficients of thermal expansion (CTE) between layers. These serve as diffusion paths for metals, as leakage current channels,

and the last but not the least, as deep-level nonradiative recombination centers that limit efficient radiative light emission^{4,5}, or at least simply reduce the net volume of active light-emitting region. Existing structures are normally manufactured using direct photolithography or e-beam lithography⁶, which is apt to damage the laminated-film structure of the devices and also generate dislocations.

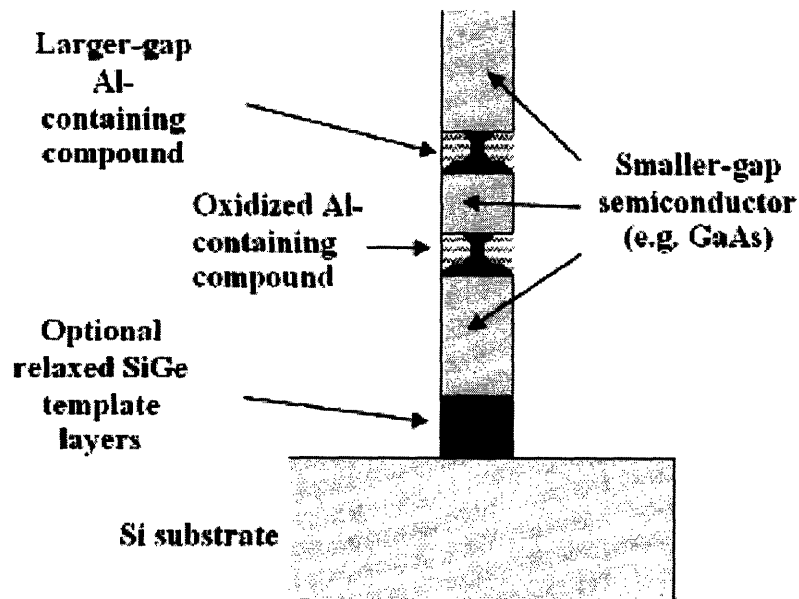
Although electrically driven compound semiconductor LEDs or LDs are already used for applications, they are costly to fabricate, because the high-quality low-defect III-V semiconductor substrates are very difficult to obtain, and thus are very expensive. For example, the size of GaAs, InP and GaN wafers available in the market is around 6 inches, 4 inches and 2 inches, respectively. Despite having smaller sizes, these wafers are still more expensive than 12-inch Si wafers. Besides, there is no volume production of substrate wafers of other compound semiconductor materials. Also, the fact that light emitting devices are usually made from compound semiconductors makes them difficult to be integrated into silicon-based systems because of large lattice mismatch.

To solve these problems, many researchers have started to investigate alternatives such as nanowire-based LEDs or LDs, especially those epitaxially grown from Si substrates, like the nanowire-array structure proposed in this thesis, which has the potential of reduced dislocation densities (and therefore improve reliability), improved extraction efficiency, and lower production costs.

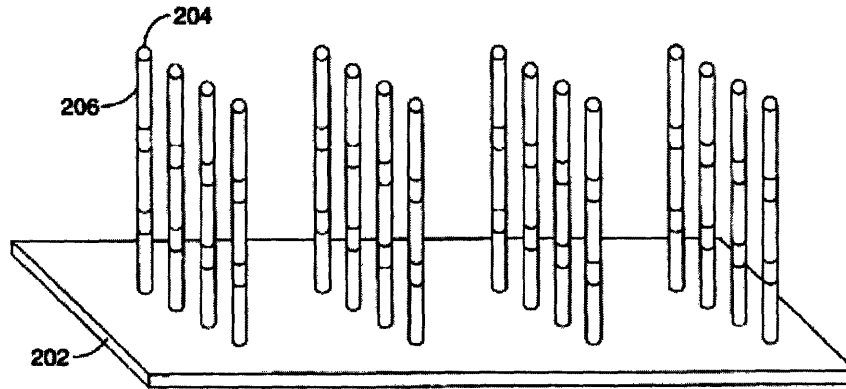
2.2. Design of the Heterostructural Semiconductor Nanowires for Light Emission

2.2.1. Features of the Proposed Design

To find an alternative for current poor-performing light emitting devices, a new idea for designing and fabricating nanowire light-emitting structure has been proposed. This section briefly discusses light emission from single heterostructural semiconductor nanowire structures, but the detailed study of the emission mechanism of the nanowire *arrays*, and the trade-off between the reliability and the performance of such fabricated nano-device structures will be found in Chapter 3 and 4.



(a)



(b)

Figure 4: Schematic structures of the proposed design for: (a)⁷ a single heterostructural semiconductor nanowire for light emission and (b)⁸ the nanowire array.

Figure 4(a) illustrates the basic idea of a single light-emitting nanowire, which is made of, but not limited to, a GaAs/AlGaAs heterostructure. Here, electrons can be confined 2-dimensionally to the small-gap material region (the central light blue part of GaAs) with the cladding of a larger-gap material (AlGaAs layers), and the oxidized Al-containing compounds functioning as barrier layers to eliminate the leakage so as to better confine the current and to create conditions optimal for stimulated emission. The active region can even be treated as a quantum dot with a 3-D confinement if the dimensions are controlled precisely. The schematic energy diagram in Figure 5 helps one to understand the confinement and emission mechanism. The GaAs quantum wire in the center contains the confined states, and the AlGaAs cladding layers function as not only the barrier for photon leakage, but also as the tunneling path to allow electrons to be injected into and extracted from the central quantum confinement region⁶ through the lower bandgap material, GaAs, that is on either side of these AlGaAs barriers.

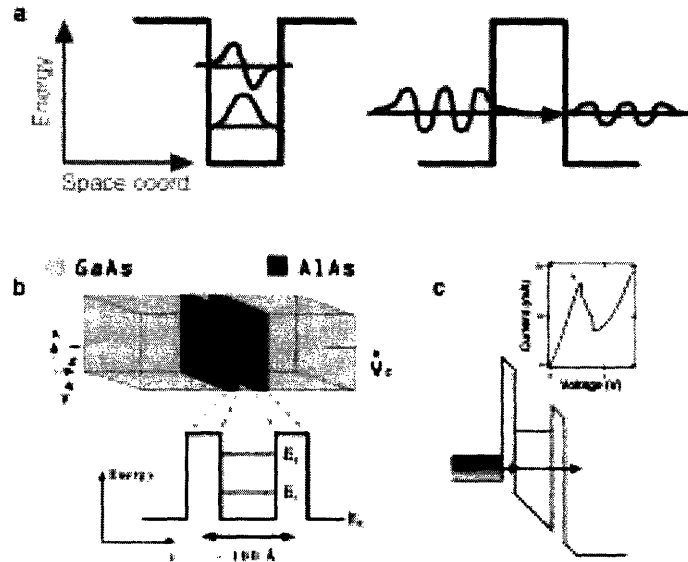


Figure 5⁶: (a) Illustrates the way attractive potential quantum wells with quantized energy levels and potential barriers for tunneling can be formed by heterostructures. (b) Illustrates the concept of a double-barrier tunneling device, in which a thin quantum layer is sandwiched between two barriers, thin enough to allow electrons to tunnel through. (c) Shows how an applied bias may bring the electrons in the emitter into and out of alignment with the quantized level in the well, resulting in a peak in the current-voltage characteristics and a region with negative differential resistance.

Feature 1:

Different from existing 2-D quantum-well LEDs or LDs, electron confinement to one or even zero dimensions offers sharper peaks of the density of states⁹. This should lead to various interesting optical properties such as “increased exciton binding, enhanced optical nonlinearities, narrower gain spectra, higher differential gain” (which gives the possibility of forming an LD with a lower threshold), “reduced threshold temperature sensitivity and increased modulation bandwidth” (Quoted from Reference 9). With a very high aspect ratio, the lasing effect can be more enhanced because of the relatively long cavity length, to acquire a higher gain [Gain= exp (gain coefficient- loss coefficient)]

$\pi L/2]$ ¹⁰, which has been experimentally proven by Justin C. Johnson *et al*¹¹. In this case, this designed structure can serve well if integrated into an LD device.

Feature 2:

The nano-scale dimensions and the inserted graded SiGe layer enable the defect-free epitaxial growth of large lattice-mismatched material layers, which can contribute to many bandgap-engineering heterostructural semiconductor devices¹². Why and how this works will be discussed in Chapter 3.

Feature 3:

Another feature with this design which must be highlighted is that different semiconductor compound nanowires can be grown from Si substrates using this concept. This will help to take advantage of commercialized large Si wafers as an alternative to epitaxial growth on small and costly compound semiconductor wafers. This also allows integration with the existing electronic and optical Si-based devices at the same chip level.

2.2.2. Experimental Result of the Light Emission from Nanowires

Many works of nanowire optoelectronics have been done by P. Yang's group, C. M. Lieber's group and L. Samuelson's group since 2000. They not only demonstrated the

outstanding light emitting effect of single nanowire made from many kinds of semiconductor materials^{11,13,14,15,16,17,18}, but also they have demonstrated fabrication of vertical-standing, highly-controlled semiconductor nanowire arrays with various geometries and better and better qualities^{19,20,21,22,23}.

Light emission in LEDs and/or LDs has been observed many, many times. Figure 6 shows the result from one of the earliest nano-laser letters published by P. Yang *et al.*¹³. Sometimes, in photoluminescence (PL) characterizations, weak LED effects can occur at a lower pumping energy (below lasing threshold) (see Figure 6A-a). The strong lasing effect (Figure 6A-b) takes place when the excitation power is above the threshold. With higher pump energy, more lasing modes (Figure 6A-c) can be observed as expected.

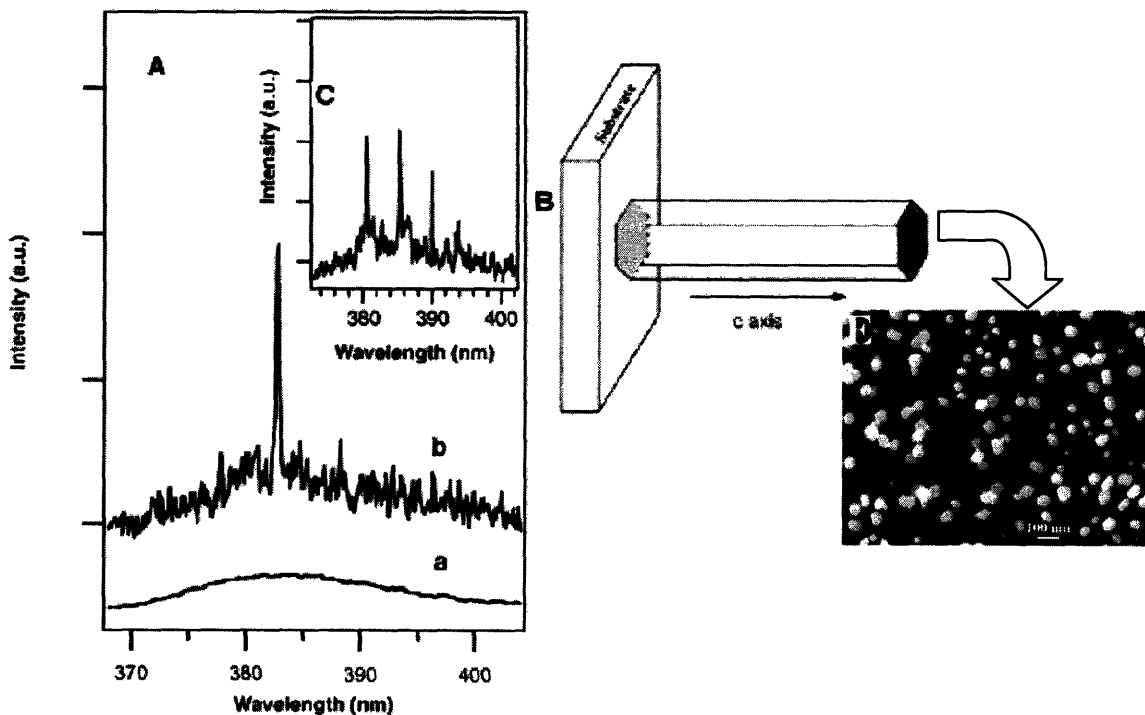


Figure 6¹³: (A) Emission spectra from ZnO nanowires on a sapphire substrate below (line

a) and above (line b and inset c) the lasing threshold. The pump power for spectra a, b and c is 20, 100 and 150 kW/cm², respectively. (B) Schematic illustration of a nanowire as a resonance cavity with two naturally faceted hexagonal end faces acting as reflecting mirrors. Stimulated emission carried out at room temperature from the nanowires was collected in the direction along the nanowire's end-plane normal (the symmetric c axis). The enlarged picture is the top-view SEM image of the nanowires.

How can this lasing action of the nanowires happen without any fabricated mirrors? As we know, to ensure stimulated emission of an LD and a concentrated light beam, a cavity must be under consideration. The resonant cavity is normally formed by either being placed into a horizontal cavity between cleaved surfaces or growing reflecting layers like a VCSEL to make a vertical cavity.

The hexagonal end planes (Figure 6B) of the ZnO nanowires grown on a sapphire substrate can be clearly identified in the SEM image, testifying the vertical growth direction. This observation combined with the observed lasing effect and the microscopic image leads to the reasonable hypothesis that the well-faceted ends can serve as the mirrors to form a natural cavity without cleavage or etching inside the wires to amplify the stimulated emission.

2.2.3. Nanowire Arrays

When nanowires come together to form an ordered array, though, optoelectronic properties extracted from the characterizations of a single nanowire maybe cannot be

simply applied to nanowire arrays, due to the possible interaction or interference amongst nanowires. Up to this point, relatively little work has been done on the topic of densely-packed nanowire arrays, so it is not clear whether such arrays can behave so as to multiply the effects of the composite individual wires, or if arrays interact as if the individual nanowires were distantly separated. Chapter 4 reports investigations on the relationship between the dimensions (the size and the separation of nanowires) and the collective properties of the array, and on the performance of nano-scaled LEDs or LDs competing with the normal broad-area (BA) light emitting devices.

Additionally, how to make good ohmic contacts to all the nanowires for efficient carrier feeding is a big challenge too, in the sense of manufacturing optoelectronic devices in such a small scale, which is still a big problem¹⁶. This is also where characterization work on nanowire array is bottle-necked, because it is very difficult to get the expected characterization result without the perfectly-contacting transparent electrodes.

The next section will quickly look at several prevalent methods of ordered heterojunctional nanowire array fabrication, which is, of course, the groundwork to make the design commercially available for good-quality device manufacturing with the desired minimum number of steps.

2.3. Heterostructural Semiconductor Nanowire Array Fabrication

Bottom-up, self-assembly processes make the dream of an accurate control of composition, position, growth orientation, dimensions, packing density and other properties of nanowire arrays a possibility, including doing so with reasonable manufacturing costs.

The traditional top-down approach based on lithography technology, dominant in the current semiconductor devices and circuit industry, limits the achievable dimensions of devices. Lithographic techniques can reproduce features as narrow as 50 to 130 nm using 193 nm Deep-UV photolithography²⁴. Implied by *Electronic Business Online 2006*, the extension to further smaller features will require converting to Extreme-UV, which will require a "major re-tooling event, with the cost for the industry running into the billions". Taking another example of writing with electronic-beam lithography, you can write features with extremely small dimensions. However, the time required to create patterns with the complexity characteristic of modern and scaled circuits is prohibitively costly for current or sub-30 nm circuit features.

The bottom-up process allows the self-assembly of nano- devices at extremely small dimensions, easily down to 3 nm²⁵. Currently, the most popular method for growth of nanowires is based on the VLSE (Vapor-Liquid-Solid-Epitaxy) mechanism. The key

issues for this method are the precise control of the flow time and rate of reactant gases, control of the reaction temperature, control of the nanowire growth direction and size, control of the facet shape, and for ordered growth, control of the growth position. For nanowires with heterostructures or superlattices, the ability to abruptly switch between gases is also important. Section 2.3 will give a rough description of current accomplishments and challenges for nanowire array fabrication.

2.3.1. Catalyst-Assisted VLSE Mechanism to Grow Nanowires Vertically

A typical VLS process (Figure 7) to grow nanowires starts from the saturation and dissolution of gaseous reactants into the nano-sized liquid metal catalyst, followed by the nucleation to form a solid phase, and then the one-dimensional growth of single-crystalline wires²⁶. VLSE takes advantage of the low eutectic temperature for a binary system, for instance, 363°C for Au-Si and 630°C for Au-GaAs (Figure 8). The feasibility that the synthesis of compound semiconductor nanowires using metal-catalyst-assisted VLSE has been demonstrated in systems with pseudobinary phase diagram²⁵ by Lieber's group as early as 1998. Single-crystalline GaAs nanowires with diameters of a few nanometers and larger can be fabricated in large amounts via *laser ablation* by achieving the required lowest reaction temperature and setting the catalyst:GaAs composition to that read from the pseudobinary phase diagram. To first order, the sizes of nanowires are determined by the dimensions of catalyst²⁷.

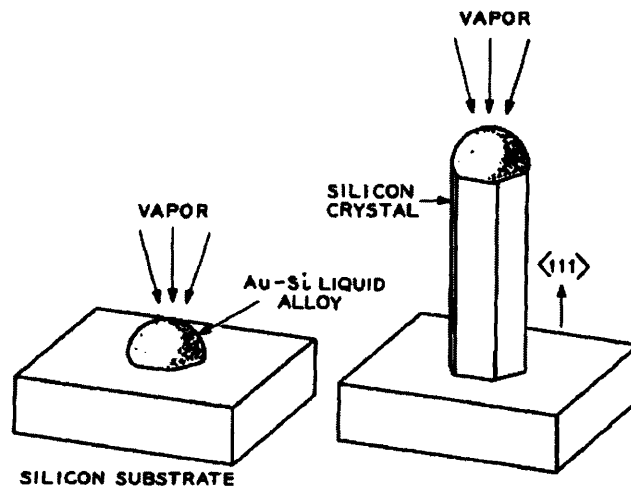


Figure 7²⁶: Schematic illustration of a Si crystal formed via VLS.

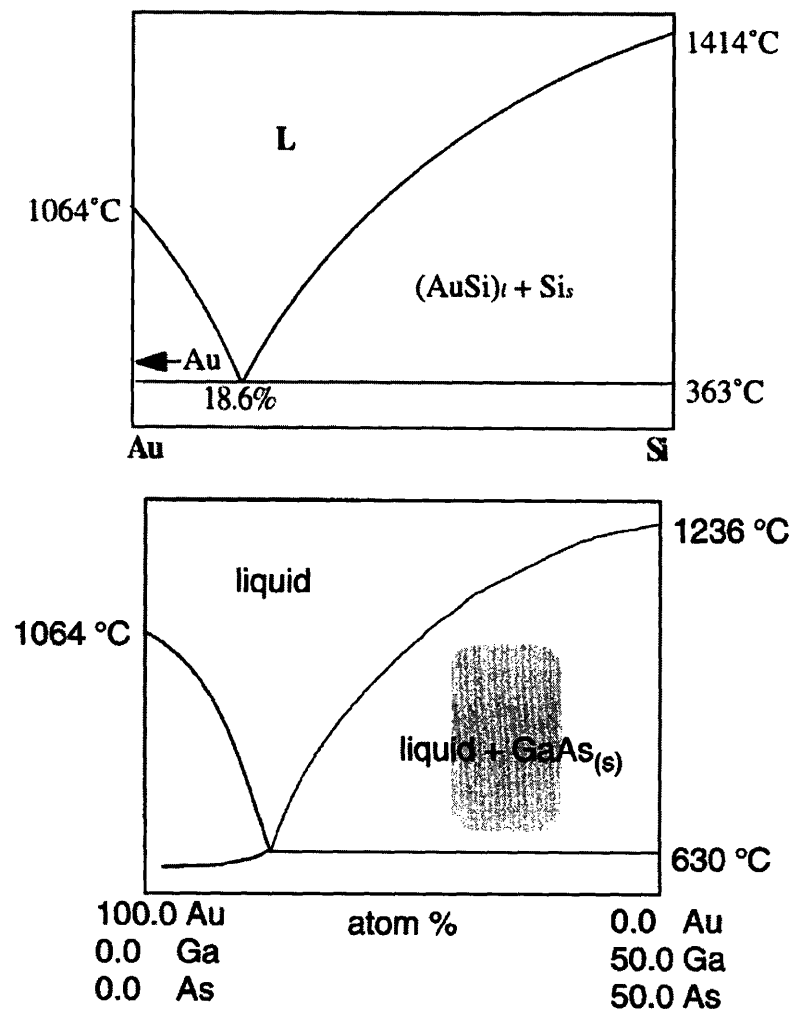


Figure 8²⁵: Phase diagrams for Au-Si (upper) and Au-GaAs (lower) systems.

2.3.2. Growth Direction and Substrate Selection

To choose the right substrate is very important, because for a vertical growth, the growth direction is determined by the crystallographic orientation of the single crystal substrate. For example, the preferred growth direction of Si nanowire is $\langle 111 \rangle$, while for ZnO it is $\langle 001 \rangle$, so $\{111\}$ single crystal Si wafer should be used for vertical growth of Si and compound semiconductor nanowires²⁶. If a (001) Si wafer was used as a substrate, epitaxial growth would occur in three equivalent $\langle 111 \rangle$ directions that are not normal to the wafer surface. For GaAs, specifically, the preferred growth direction is also $\langle 111 \rangle$, with the shape of the $\{110\}$ sidewall facets of hexagonal nanowires grown from the symmetric (111)B GaAs substrate.

Recently, several experiments have proven the diameter-dependent growth direction of Si. In recent experiments there is some evidence that while larger-diameter nanowires prefer to grow along the $\langle 111 \rangle$ direction, very small-diameter nanowires grow mostly along the $\langle 110 \rangle$ direction²⁸. Silicon nanowires grown epitaxially on Si (100) change their growth direction from $\langle 111 \rangle$ to $\langle 110 \rangle$ at approximately 20 nm in diameter²⁹. U. Gosele *et al.* suggested that the “interplay of the liquid-solid interfacial energy with the silicon surface energy expressed in terms of an edge tension is responsible for the change of the growth

direction”.

Yang's group found that the substrate can also affect the shape of the nanowires²⁰. They demonstrated that the epitaxial growth of wurtzite gallium nitride on (100) γ -LiAlO₂ and (111) MgO single-crystal substrates resulted in the selective growth of nanowires in different directions, leading to wires with triangular and hexagonal cross-sections, respectively, and with considerably different optical emission characterizations.

2.3.3. Heterostructure Nanowire Growth

Basically, there are two types of nanowire heterostructures: axial and radial, corresponding to longitudinal superlattice and core-(multi)-shell/sheath structures. Figure 9 schematically shows the two types of heterostructure synthesis: axial (longitudinal) (Figure 9c) and radial (core-shell/sheath) (Figure 9d). Figure 9a and 9b are the same as Figure 7, and a change in the gas precursor can lead to either (c) or (d), depending on which types of sites incorporation the gas reactant is favored: (c) at the catalyst or (d) uniformly on the cylinder sidewall.

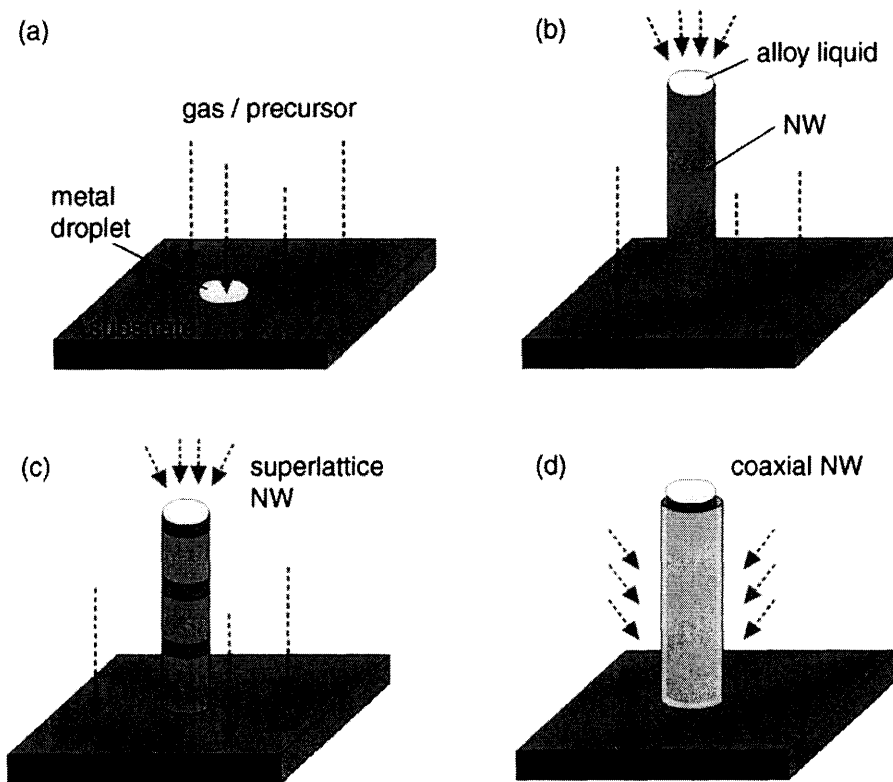


Figure 9³⁰: Nanowires of different structures based on the “bottom-up” growth mode: a) Exposure of a metal-droplet-coated substrate to reactant precursors; b) a monophase nanowire grown outwards, with the metal droplet acting as catalyst; c) a superlattice nanowire grown by consecutively alternating the reactant precursors; d) a coaxial nanowire formed by conformal coating of the preformed nanowire in (b) with a different material.

Figure 10A below shows the schematic block-by-block growth process of heterostructural nanowires of Si/SiGe by controlling the flow of gas sources, simply using the VLS mechanism. Similarly, the proposed GaAs/AlGaAs nanowire can be fabricated through the same sort of process, followed by a timed oxidation step to form the current-blocking barriers.

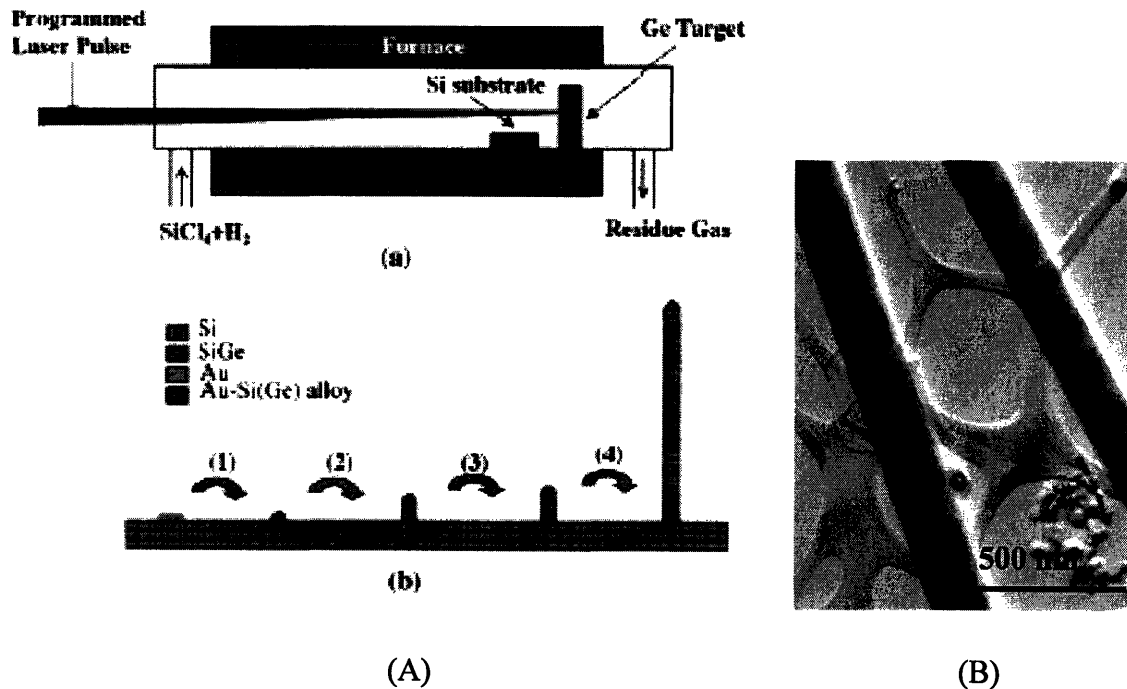


Figure 10: (A) Schematic growth process³¹ and (B) TEM images²⁷ of the block-by-block growth of Si/SiGe longitudinal heterostructure (superlattice) nanowires.

2.3.4. Nanowire Array

There are different means of making nanowire arrays. As summarized in the review article *Semiconductor Nanowires: from Self-organization to Patterned growth*³⁰, the growth control methods of both top-down and bottom-up technologies include, but are not limited to, photolithography or e-beam lithography, manipulation of single nanodots, arrangements of Au nanocrystals from suspensions, nanosphere lithography (NSL), Au deposition masks based on porous alumina--- anodized aluminum oxide (AAO), nanoimprint lithography (NIL), block copolymers for nanolithography and crack lithography. NIL appears to be very promising because “it is in many respects capable

of producing structures comparable to, or even smaller than, those of e-beam lithography but at considerably lower cost and with much higher throughput”. Figure 11 and Figure 12 are SEM images of nanowire arrays of different materials made using different fabrication method.

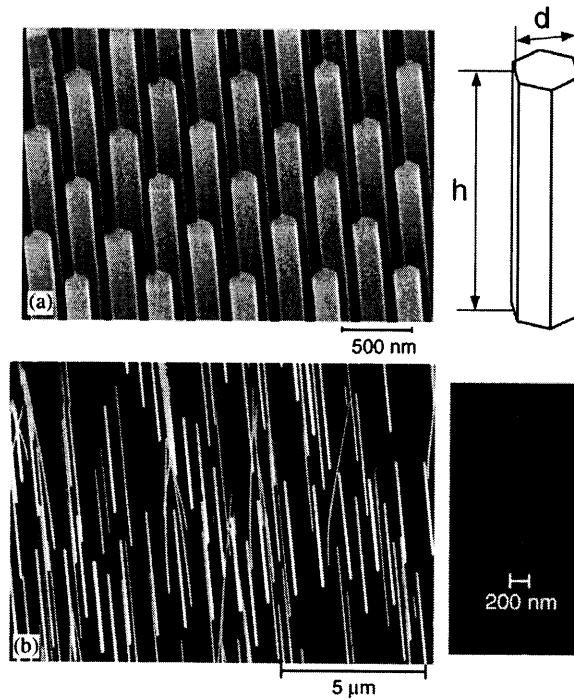


Figure 11³²: Typical Bird’s eye SEM image of ordered GaAs nanowires through patterned SiO₂ via catalyst-free growth: (a) extremely uniform arrays of nanowires with wire diameters around 200nm, and (b) smaller and longer, but less uniform nanowires.

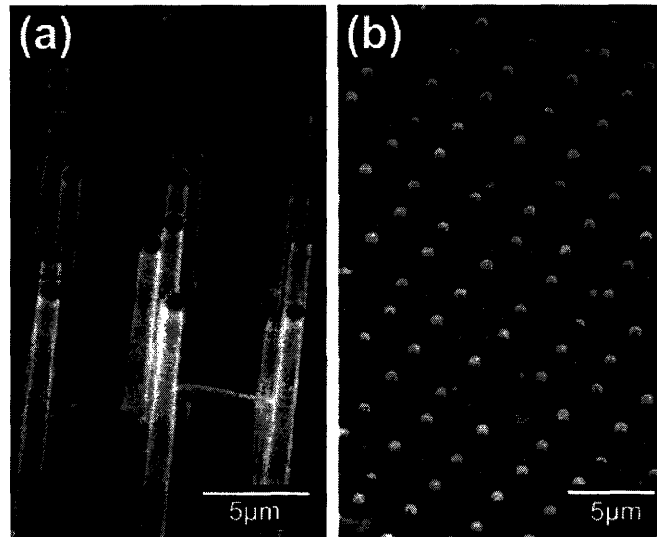


Figure 12³³: (a) Array of silicon nanowires, with 5 um pitch, deposited by CVD of $\text{SiH}_4\text{:HCl:H}_2$ at 800 °C; (b) Array of integrated gate silicon nanowire cathodes fabricated using the self-aligned process templated by the porous alumina (AAO).

2.3.5. Patterning, Template Manufacturing and Dewetting Technology

Patterning is an important step prior to controlled selective growth, which is of great interest for industrial applications, especially those with small scales down to the nanometer range. An inexpensive means to pattern large areas on the square-centimeter scale³⁰ and beyond is needed. Ordered metal catalyst arrays for nanowire growth can be realized by nanopatterning. Therefore, nanopatterning techniques become essential when position-control of spatially-separated nanowires is desired.

K. Hiruma *et al.*^{34,35} working in Hitachi obtained small Au particles formed from a thin evaporated Au film, which “broke up during annealing and reshaped into nano-scale droplets”. This particle forming process is called dewetting, and can be templated to

form very uniform metal-catalyst arrays^{36,37}.

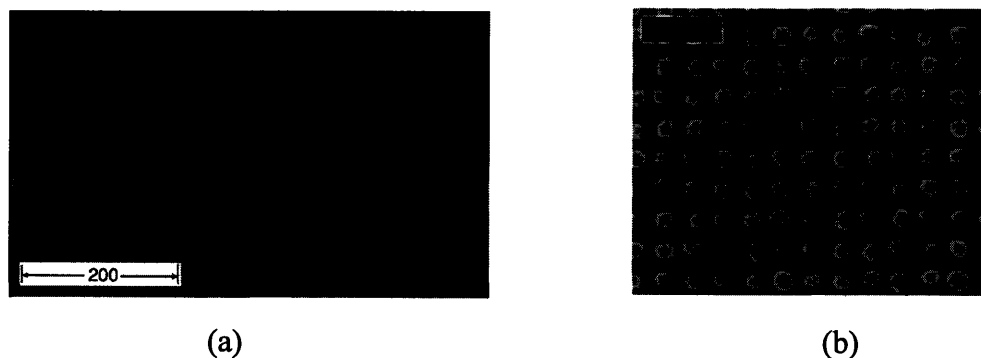


Figure 13³⁷: (a) SEM Topographic templates of a square array of inverted pyramids in (100) silicon; (b) Ordered arrays of one particle dewetted per pit for Au catalyst.

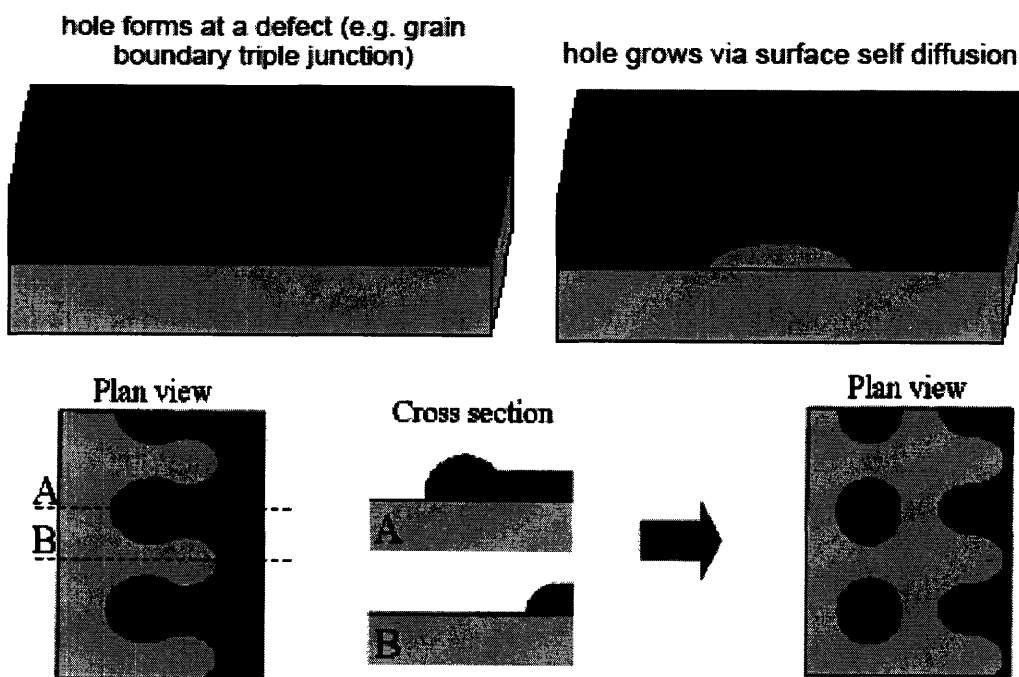


Figure 14³⁸: Dewetting process without templating.

In dewetting of flat polycrystalline films, grooves form at grain boundary triple junctions in order to minimize the interfacial energy associated with grain boundaries and surfaces.

If the grooves are deeper than the film thickness, holes form, exposing the substrate-ambient interface. Dewetting occurs through growth of these holes, often through self-diffusion on the film surface, leading to the formation of islands around the perimeter of the hole and then further unstable growth³⁶. Films deposited on substrates with regular topographic features will dewet in a controlled way, leading to ordered nanoparticle arrays³⁷.

2.4. Chapter Summary

This chapter went through the background theories and technologies behind the proposed nanowire array design. The features of the design will be further examined in Chapter 3 and 4 after all the interlinked pieces are understood, such as the light-emitting mechanism in a heterostructural nanowire and the fabrication method of the uniform as-proposed templated heterostructural semiconductor nanowire array.

Chapter 3 Reliability Investigation

In this chapter, we discuss why dislocations are difficult to nucleate in nanowires, what the critical radius of nanowires grown epitaxially is, and how dislocations are going to move or be hindered from motion, all of which affect the reliability and lifetimes of optical devices. Dislocation densities are expected to be reduced in nanowires. However, when the light generation area, i.e. the active region area, is getting much smaller than normal LEDs or LDs, there might be interference between light extraction from individual nanowires. Whether the efficiency of light emission and the performance in terms of output light power decline will be investigated in the next chapter.

3.1. Misfit Dislocations and Threading Dislocations

Basically, there are two types of dislocations which can form during epitaxial growth: misfit dislocations and threading dislocations³⁹. Misfit dislocations start to nucleate when the dimensions of the epi-layer exceed certain values, which are said to be a *critical thickness*⁴⁰ and a *critical radius* (for nanowires)⁴¹. Misfit dislocations will not impact on the lifetime or reliability of devices if they lie within the interface without pushing any defect into the active region.

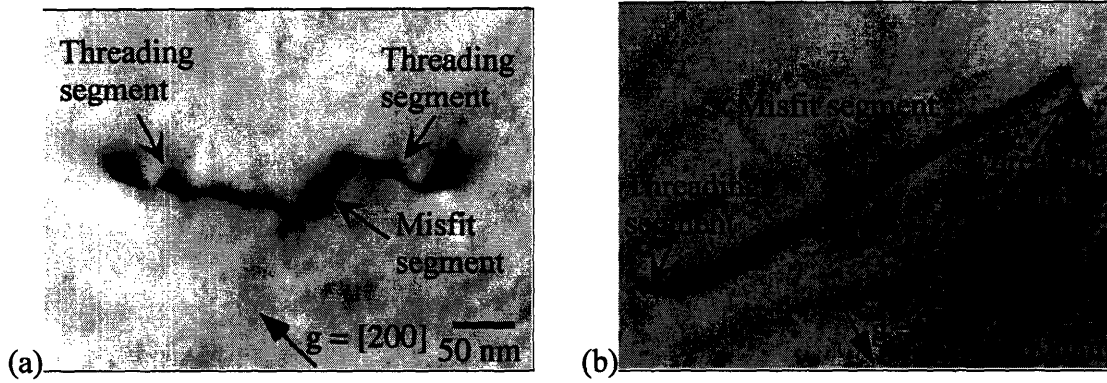
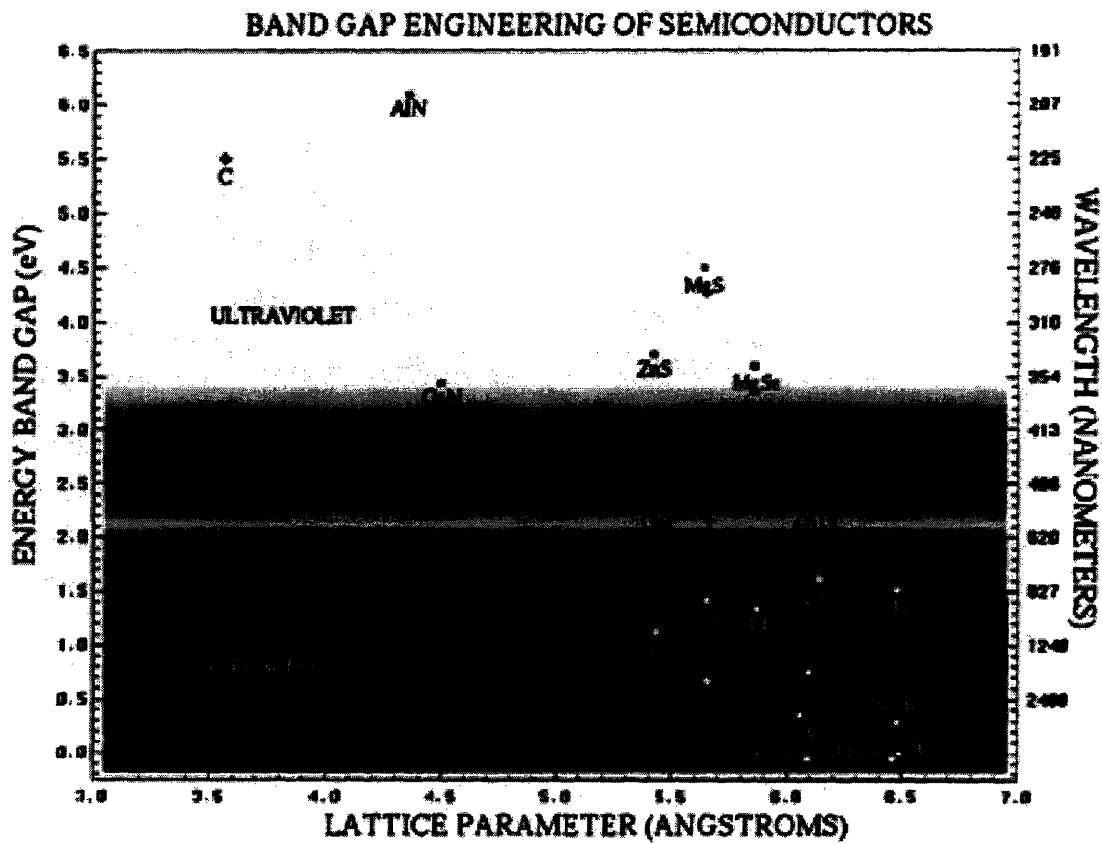


Figure 15⁴²: Misfit dislocations and threading dislocations in GaAs/In_{0.2}Ga_{0.8}As/GaAs: (a) misfit segment at In_{0.2}Ga_{0.8}As layer thickness of 4 nm; (b) elongated misfit segment at In_{0.2}Ga_{0.8}As layer thickness of 10 nm.



proposed by this thesis, it is obvious that AlAs, AlGaAs, GaAs and Ge are almost all lattice-matched, but with a 4% mismatch with Si (The lattice parameters for GaAs or Ge and Si are 0.565 nm and 0.543 nm.). This is to say that it is very easy to epitaxially grow high-quality GaAs/AlGaAs structure on a GaAs or Ge substrate without any misfit. On the other hand, it is very difficult to grow low-defect structures on a Si substrate in conventional bulk structures. Whether this amount of mismatch can be accommodated elastically without forming a misfit dislocation in a nanowire will be discussed in Section 3.2.

Threading dislocations usually come from the substrate or as the trailing portion of a misfit dislocation loop, and become more mobile and able to thread in the active region, due to elevated activation energy, which is termed the Recombination Enhanced Defect Reactions (REDR)⁴⁴. Upon operation of devices, the existing threading dislocations or other defects can act as trap states enabling the nonradiative recombination of carriers leading to conversion of the energy to vibration energy. The released nonradiative energy can then lower the energy barrier for diffusion of point defects, leading to dislocation climb, possibly resulting in movement into the active region. The term Dark Line Defects (DDL) arises from the appearance of dislocations as nonradiative recombination regions, giving rise to reduced gain under photoluminescence or electroluminescence imaging⁴⁵. The DLD network grows from a single dislocation initiating from the substrate threading through the active region, during the structure

growth process.

Consequently, although the injected carriers are collected and confined in the lower bandgap GaAs active region, the dislocation density, especially the threading dislocation density, must be reduced as low as possible. There are some approaches that have been developed to decrease the concentration of threading dislocations. A very effective method is to grow a thin superlattice of graded layers between the film and the bulk substrate, which can be adapted for use with nanowire heterostructures, as shown as the green part in the schematic diagram of the proposed design (Figure 4). The mechanism can be illustrated in the figure below:

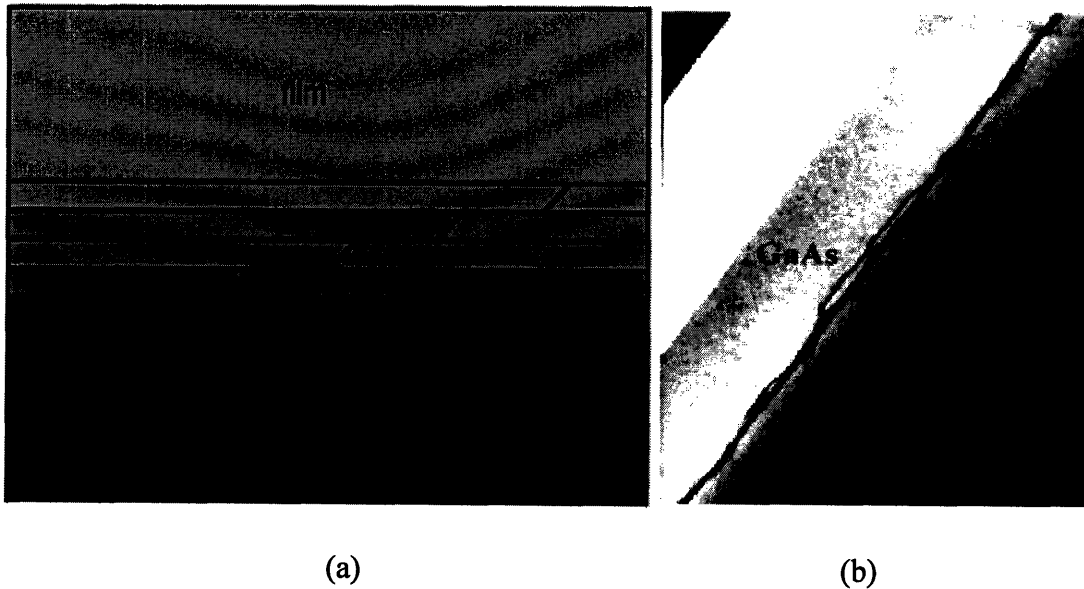


Figure 17⁴⁶: (a) Schematic drawing showing the slip of threading dislocations across the graded thin layers; (b) Cross-sectional TEM image of GaAs/Ge/Si_{1-x}Ge_x/Si. The GaAs, Ge and the top graded SiGe layers are shown.

The threading dislocations propagate at interfaces to form misfit dislocations. They

easily slip across the thin superlattice layers because of the “reduced drag force” on a *compliant substrate*⁴⁷. It was concluded that threading dislocations moving at a lower film thickness, i.e. at the graded SiGe layers in the proposed design, have a lower probability of interacting and multiplying, and therefore slip across longer distances, thus relaxing a larger film area. Since the in-plane area is nano-scale, the termination of threading dislocations at the surfaces will be very likely to achieve after the slip. No new dislocations nucleate during this relaxation process, leading to a final state with a lower remaining threading dislocation density.

This given example in Figure 18 is for GaAs lasers fabricated on improved Ge substrates⁴⁸ (E. A. Fitzgerald *et al.*), and supports the improved reliability obtained using the inserted graded SiGe layer to reduce the dislocation density in the structure. By examining the lifetime of GaAs quantum well devices on Ge/GeSi/Si, the much better failure test result [the failure is due to the recombination-enhanced defect reactions (REDR), which is consistent with L. C. Kimerling *et al.*⁴⁴] strongly supports the explanation of TD relaxation and defect elimination in the *improved device* resulting from inserting a graded SiGe layer between the Si substrate and overlayer films.

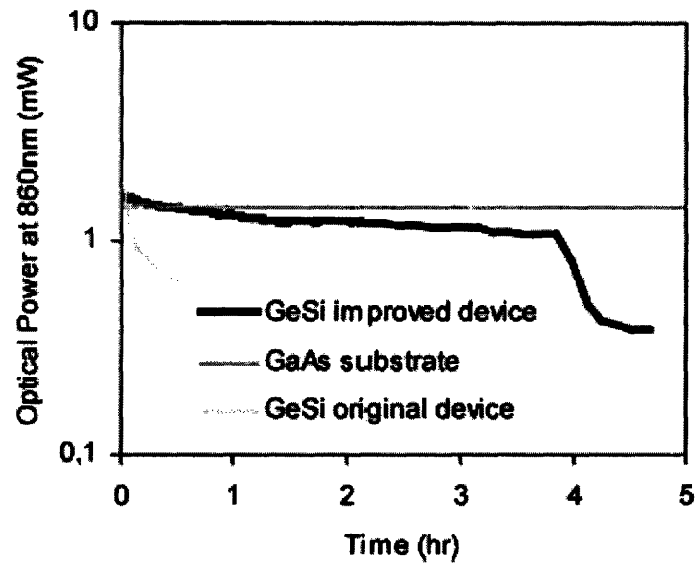


Figure 18⁴⁸: Lifetime measurements showing laser optical power vs. operating time for improved GaAs/AlGaAs quantum well laser structures fabricated on Ge/GeSi/Si substrates. Laser performance data for previously reported first-generation device structures on Ge/GeSi/Si and GaAs substrates is included for comparison.

Alternatively, other than decreasing the threading dislocation density inside the structure due to the graded layers, the nanowire *array* arrangement can be treated as another TD-reducing feature of the proposed design. As imagined, a device constructed with a nanowire array structure will have a very high probability to continue to work, even if a few nanowires degrade due to the propagation of threading dislocations at working temperatures upon device operation, because no chain-reactions of dislocation movement or nucleation can happen with the separation between nanowires. However, this has not yet been proven through experiments.

3.2. Critical (Core) Radius and Critical Shell Thickness

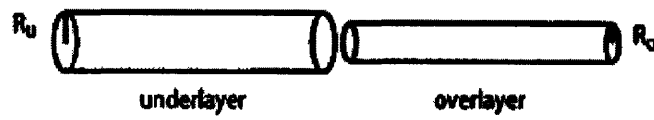
In nanowires, a low probability of the presence of misfit dislocations at the heterojunctions can be accounted for by the small area of the interface⁴⁹, on the order of less than 100 nm², and the strain relaxation in the lateral direction perpendicular to the nanowire growth direction⁴¹.

The *critical thickness of films* has been studied by many, many scientists, among which the criterion most researches still look at and want to improve on, is the Matthews-Blakeslee Model (M-B Model)⁴⁰. Numerous studies have been done both experimentally⁵⁰ and theoretically⁵¹, ever since M-B Model was advanced. Here, to show the difference of the dislocation evolution between the nanowire growth and thin film epitaxy, only the critical radius of nano-scale wires will be discussed, as a function of the lattice mismatch, after which the critical shell thickness will also be considered (for the case of core-shell structures).

For calculation of the critical (core) radius, U. Gosele *et al.* (2004) and E. Ertekin *et al.* (2005) worked out similar results: the former one is five times larger than, and the latter one roughly an order of magnitude larger than the critical thickness of the corresponding thin-film/substrate material system. The former group used the force equilibrium method, considering the “loss” and “gain” resulting from the motion of a threading

dislocation moving in the slip plane of a thin layer strained by certain misfit with a bulk substrate⁴¹, and the latter compared the fully elastically accommodated misfit strain energy with the sum of the residual elastic strain energy and the misfit dislocation energy in a semi-coherent (incoherent) system¹². Both groups came to the conclusion that the critical radius decreases with increasing lattice mismatch.

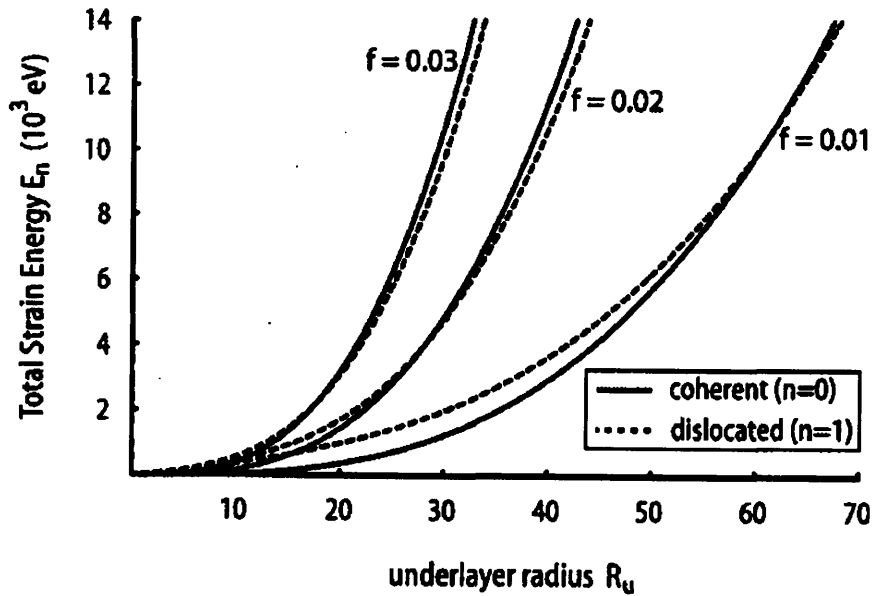
Unbonded:



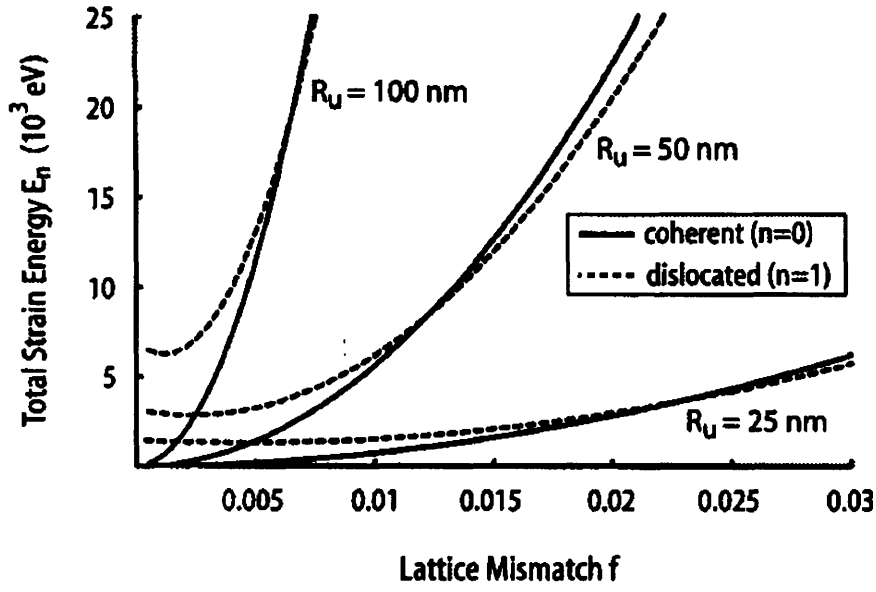
Bonded:



(a)



(b)



(c)

Figure 19¹²: (a) Schematic diagrams of heterostructured nanowire, before and after interfacial bonding. Energy E_n [$n = (0,1)$], indicating the presence of zero or one dislocation, versus: (b) underlayer radius R_u with lattice mismatch $f = 0.01, 0.02, 0.03$; (c) lattice mismatch f with underlayer radius $R_u = 25, 50, 100$ nm, taking the Burgers vector value b as 0.23 for nanowire heterostructures.

In Figure 19, the schematic drawing of the bonded overlayer and underlayer nanowires resemble the heterojunctional nanowires considered in this thesis. This tells us that for underlayer radius $R_u = 25, 50, 100$ nm, the largest mismatch that can be elastically accommodated cannot exceed 2.4%, 1.2%, 0.6%; for $f = 0.01, 0.02, 0.03$, the critical radius is found to be 61, 28, 17 nm. By comparison, the critical thickness of the same material system in thin-film/substrate case is $h^* = 2.86, 1.07, 0.55$ nm, for $f = 0.01, 0.02, 0.03$, respectively.

E. Ertekin *et al.* further took the Burgers vector dependence into account and thus

suggested that the critical radius depends more on the specific material system rather than simply on the mismatch or the lattice parameters.

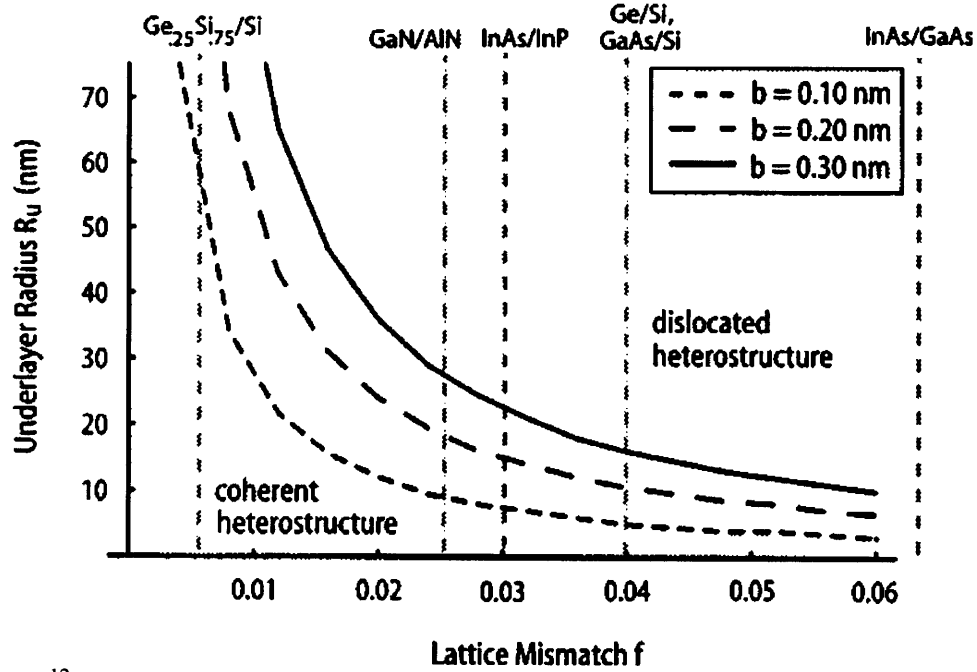


Figure 20¹²: Equilibrium diagram illustrating regions in (f, R_u) space for which the coherent and dislocated nanowire heterostructures are stable with respect to each other. Take different materials and different Burgers vectors into account. All the other parameters are the same as in Figure 19. The vertical lines are drawn to correspond to the lattice mismatch associated with some common heterostructure systems. For $f = 0.04$, $R_u = 15, 10$ and 5 nm for $b = 0.3, 0.2$ and 0.1 nm. Extrapolating from the $b = 0.3$ nm curve for $\text{Ge}_{0.25}\text{Si}_{0.75}/\text{Si}$ system with $f = 0.006$, the critical radius is much larger than 100 nm.

Figure 20 again indicates that when R_u of a nanowire is small, the strain can relax laterally, and thus a large mismatch f can be coherently accommodated. Specifically for the epi-system of GaAs or Ge on Si(111), for the sake of simplicity, we take the Burgers vector to be a perfect 90 degree dislocation as $1/2(110)$, and b value is then ~ 0.39 nm. This curve of $b = 0.39$ nm was not drawn in the plot above, but the corresponding critical radius for 4% mismatch can be approximated as 20 nm. Since the actual mismatch for

the proposed structure should be between the graded SiGe layer and Si substrate, rather than in between GaAs and Si, so the value of f substituted could be much smaller, leading to a critical radius much larger than 20 nm. The more accurate critical value depends on the specific materials system (composition, lattice constant and crystal structure) and the specific Burgers vector, but it is very possible to achieve a critical radius $\gg 100$ nm for a slowly-graded SiGe/Si system.

U. Gosele *et al.* got a smaller result of R_c than Ertekin's result and the difference was explained by U. Gosele *et al.* as taking the local minimum criterion instead of the zero total energy used by Ertekin *et al.*

Ertekin reported that no misfit dislocations have yet been observed in nanowire heterostructures so far. U. Gosele and G. Kastner gave a reasonable explanation of why nanowires are free of dislocations with R well above R_c . They brought forward three difficulties encountered when forming a dislocation in a nanowire: the high energy barrier for the nucleation of a half-loop; the elastic boundary condition of zero cross-sectional shear stress at the surface of the nanowire; and the low density of crystal defects (or even free of defects) that can act to catalyze dislocation nucleation in nanowires.

A quantitative calculation was given by S. Raychaudhuri and E. T. Yu recently, indicating

a unique critical shell thickness, dependent on core radius in the GaN/Al_{0.5}Ga_{0.5}N core-shell system⁵².

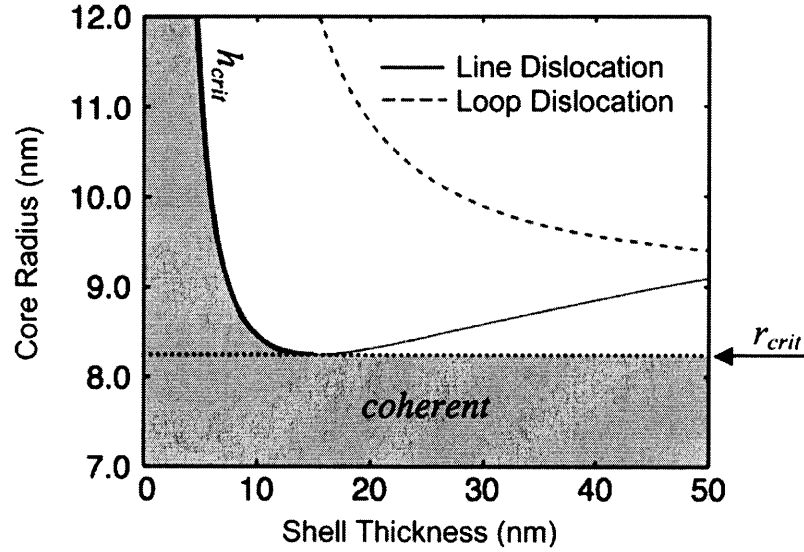


Figure 21⁵²: Plot of the critical dimensions calculated for a coaxial nanowire structure comprised of a GaN core and Al_{0.5}Ga_{0.5}N shell. The shaded region of the plot shows all possible strained coherent geometries, which are quantified by a critical core radius r_{crit} and the critical shell thickness curve h_{crit} .

There is a critical core radius R_c of 8.2 nm, below which a coherent coaxial nanowire will always exist, regardless of shell thickness. Such a critical core radius exists because of the distributed strain between the core and shell. Since the core volume is constant, the strain energy of the system stored inside the core will no longer increase with shell thickness after certain point. If the core volume is sufficiently small, the strain energy stored inside the core will never be high enough to activate the formation of a dislocation.

Hence, in a word, the critical dimensions of a core-shell nanowire structure can be

defined by a critical core radius below which dislocations will never form and a critical shell thickness that is dependent on the core radius. Basically, no dislocation forms below the calculated critical radius, which is 5 to 10 times higher than the critical thickness of the comparable thin film system, and in many cases, no dislocations are observed even beyond the critical radius for nanowires due to reasons given by Gosele and discussed above.

3.3. Chapter Summary

The good reliability of heterostructural semiconductor nanowire arrays can be expected due to three reasons:

1. Elastic relaxation via lateral strain relief is possible, so that the need for strain energy reduction by misfit dislocation formation is reduced, so critical dimensions are increased.
2. Even with the existence of dislocations, the density of threading dislocation can be reduced to a much lower level by relaxation across graded layers.
3. No chain-reactions of dislocation movement or nucleation can happen with the separation between nanowires, so that light-emitting arrays can continue to function, even if a few nanowires degrade.

However, none of these effects on nanowire arrays have experimentally demonstrated.

In sum, nanowires with dimensions in the range of $R \sim 20$ nm for a misfit = 4% (e.g. for Ge on Si with $b = 0.39$ nm) and $R \sim \gg 100$ nm for a misfit $\leq 0.6\%$ (e.g., $\text{Ge}_{0.25}\text{Si}_{0.75}/\text{Si}$ and SiGe/Si with less Ge composition) are likely to form defect-free structures, so that their reliability compared to film-based devices should be greatly improved. It is also important to note that these radii set a lower, but safer, limit for the true radius below which wires will be defect free, as nucleation and multiplication mechanism may not operate until larger radii are reached.

Chapter 4 Evaluation on the Light-Emitting Performance of Nanowire Arrays

As dimensions go down to the nano- scale, reliability can be highly improved, as discussed in Chapter 3. However, careful research on the optoelectronic performance of such fabricated nano-scale light-emitting device has not been done.

People may have doubts regarding the advantages of the light-emitting properties of nanowire arrays. For example, with a much higher density of surface states and relative smaller junction areas compared to their bulk counterparts, will the light power be less than the broad-area devices with equivalent chip areas? Will the improved reliability of nanowires be traded off for a reduction of the quantum efficiency or optoelectronic performance? Also, the effects of nanowire spacing and the packing density should be investigated too.

In this chapter, a discussion will be brought out to answer the question of whether the proposed nanowire-array LED or LD performs better than, or at least the same as, conventional broad-area LEDs or LDs, or alternatively, if the light-emitting properties of nanowire arrays are degraded with respect to current broad-area devices, and therefore whether it is worth the penalty of the degraded performance for the highly desired

improved reliability. What's more, if we demonstrate that the performance of a nanowire array is able to compete with broad-area devices, the relationship between the light-emitting properties and the dimensions of the wires and the spacing in between must be investigated in the future research.

4.1. Degraded or Improved Internal Quantum Efficiency?

4.1.1. Degraded?

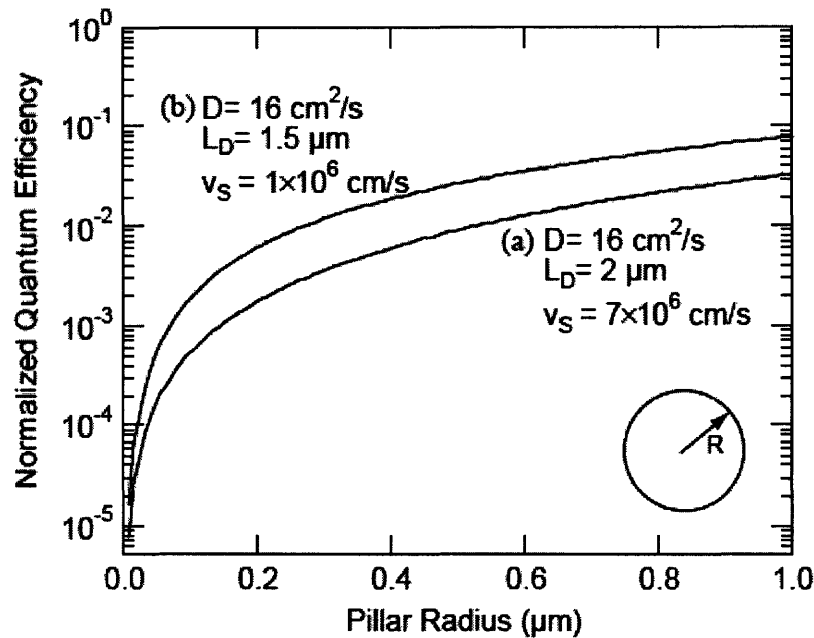


Figure 22⁵³: Effect of surface nonradiative recombination on the photoluminescence efficiency in pillar structures. (a) and (b) roughly correspond to the weak and strong excitation regime.

A theoretical calculation of the normalized PL intensity $I(R)/I(\infty)$ is plotted versus the radius R of a GaAs/AlGaAs axial heterostructure in Figure 22⁵³. Considering the small

diameter of the nanowires, the significant influence of surface states as non-radiative recombination sites might be expected to cause a dramatic decrease of the efficiency.

4.1.2. Passivation Effects

The nano-scale and high aspect ratio of nanowires leads to a high density of surface states, due to the large number of dangling bonds associated with the large surface area. This can cause severe degradation of optoelectronic device performance due to non-radiative recombination.

Experimental evidence from many research groups has shown that the core-shell nanowire structures can efficiently passivate the surface states of bare nanowires.

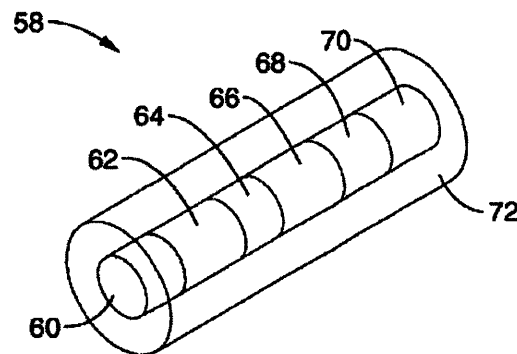


Figure 23⁸: The schematic of a heterostructural nanowire cladded radially by a shell.

Justin C. Johnson's group⁵⁴ (2003) showed that their measured PL intensity above the lasing threshold for GaN/AlGaIn core (5 to 40 nm in diameter)/shell (50 to 100 nm in thickness) nanowires is higher than that for pure GaN nanowires by almost an order of magnitude. However, it is still lower than that for many other types of GaN microstructures, which is attributed to the reduction of the gain volume by several orders than other lasing cavities in GaN microstructures. W. D. Yu *et al.*⁵⁵ (2005) found the PL intensity for SnO₂ nanowires (50 to 100 nm in diameter) coated with ZnO nanocrystals to be as high as 13 times as that for pure SnO₂ nanowires. L. Samuelson's group⁵⁶ (2005) showed an improvement of the emission efficiency 2 to 3 orders of magnitude of GaAs/GaInP core (60 nm in diameter)/shell (70 to 100 nm in thickness) nanowires compared to bare GaAs nanowires.

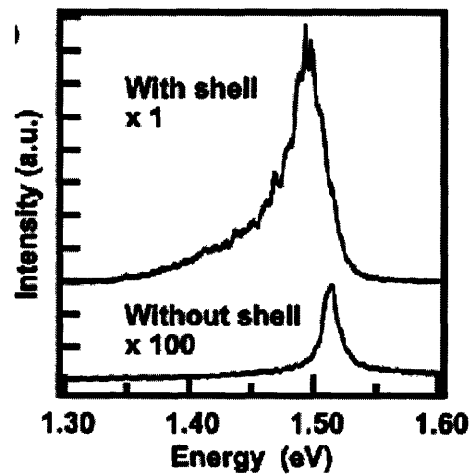


Figure 24⁵⁶: PL performed at 5 K from 60 nm nanowires with and without the shell. The shell improved the emission efficiency 2 to 3 orders of magnitude.

Samuelson tested the PL intensity of nanowires having the core radii of 10 nm, 20 nm and 30 nm with shell thickness 70 to 100 nm. Strong luminescence was observed for all the shelled nanowires, and only the 30 nm bare GaAs wire has the luminescence detectable (but still $\sim 10^3$ times lower than the shelled one as shown in Figure 24)⁵⁶. A more close-up look comparing Figure 22 and Figure 24 reveals that the 10^3 improvement is quite exciting considering the 10^4 to 10^5 degradation of efficiency for the nanowires with radii less than 50 nm. Therefore, due to core-surface passivation, the internal efficiency of nanowires is not necessary to be significantly degraded by the surface effect, while at the same time, the nanowires can still benefit from the defect-free epitaxy and the improved reliability at nano- scales.

Another more detailed example is W. I. Park's investigation of the shell-passivation effect⁵⁷ as illustrated in Figure 25 and Figure 26. The inset in Figure 25 indicates the highest PL intensity peak at a shell thickness of 13 nm for the nanowires having the same core radius of 9 nm. The research group said that for the shell thickness up to 13 nm, the passivation of the surface states and the increased excitation volume for thicker heterostructures can explain the increasing trend; and for the shell thickness over 13 nm, another radiative transition in $\text{Zn}_{0.8}\text{Mg}_{0.2}\text{O}$ or the nonradiative recombination at dislocations formed beyond the critical shell thickness would explain the small decreasing trend (but with results that are still better than for pure ZnO nanowires).

Figure 26 characterizes the stability at different temperatures of core-shell ZnO/Zn_{0.8}Mg_{0.2}O, thin ZnO and thick ZnO nanowires. The core-shell structure shows obvious superior stability.

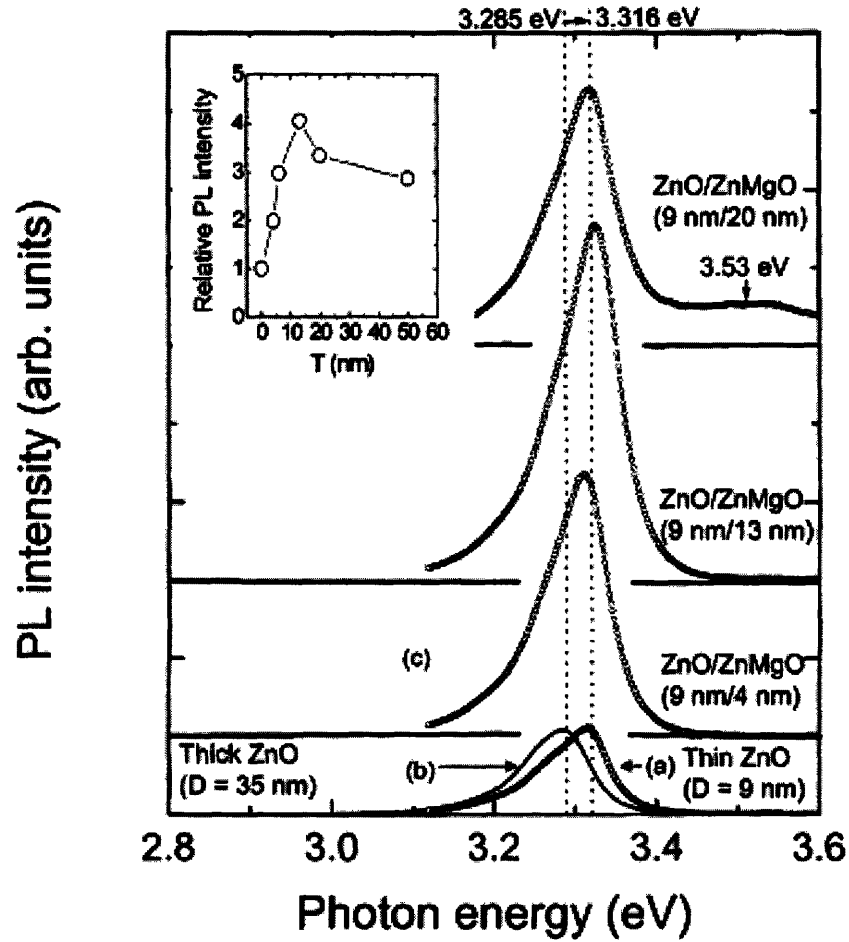


Figure 25⁵⁷: Room-temperature PL spectra of ZnO nanorods with average diameters of (a) 9 and (b) 35 nm, and (c) ZnO/Zn_{0.8}Mg_{0.2}O coaxial nanorod heterostructures. The inset shows the normalized PL intensity of near-bandedge emissions, depending on the Zn_{0.8}Mg_{0.2}O shell layer.

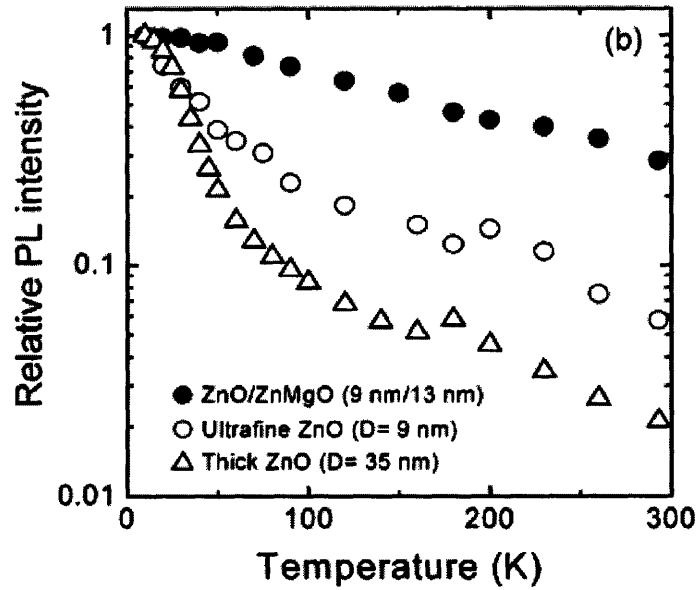


Figure 26⁵⁷: Integrated PL intensity normalized with the PL intensity at 10 K as a function of temperature for shell thickness = 35 nm and ultrafine ZnO nanorods and ZnO/Zn_{0.8}Mg_{0.2}O coaxial nanorod heterostructures.

However, more details about the radial epitaxial cladding to form a core-shell structure to passivate the surface states of nanowires should be studied in the future, such as the efficiency of the passivation, the quantitative calculation of how much improvement could be expected, and the influence on the maximum obtainable nanowire packing density.

To passivate the surface states, some other ways have also been tried, such as thermal treatment in hydrogen to make hydrogen-terminated bonds for ZnO and Si nanowires^{58,59}, and use of transparent insulating materials, those of which should easily fill the gaps among the nanowires, endure the heat in a follow-up annealing process or the like and

not disturb light emission⁶⁰, such as spin on glass (SOG: a kind of transparent dielectric material)⁶¹, SiO₂ or epoxy resin for GaAs and GaN nanowires. Also indicated by Reference 60, the transparent insulating layer is preferred to form slightly lower than the height of the nanowires so that the top ends could be connected to the transparent electrodes (e.g. ITO), otherwise an etching process might have to be involved to expose the top ends. Yet which method is the best is still unknown.

In the case that an epitaxy cladding is needed for passivation, it must be pointed out what fraction of the total device area would be sacrificed to:

- a) the use of wires with spacing in between, instead of a continuous film;
- b) the need to add cladding;
- c) the need for there to be sufficient wire spacing to coat the wires with cladding;
- d) assuming all of these is done with wires below the critical dimensions [core radius smaller than ~100 nm] for reliability improvement.

4.1.3. Improved?

In contrast with the discussion in Section 4.1.1, there are some reports suggesting that nanowires might have an *improved* internal quantum efficiency compared to broad-area devices.

H. W. Choi *et al.*⁶² (2005) measured the 1 cm^{-1} Raman shift to demonstrate that only in sub-micron down to nano- scale can significant strain relaxation take place in arrayed LEDs. Partial or complete strain relaxation in nano- LEDs will lead to the reduction of the *piezoelectric field*⁶³, and an incremental increase in the light-generation area, which should both lead to an increase in the internal quantum efficiency.

However, it should be noted that the amount of improvement of internal quantum efficiency may not be large enough to compensate for the huge loss due to high density of surface states (even with the passivation effect).

4.2. Improved Extraction Efficiency and Increased Output Power Density

No in-depth work has been done in this area for the nanowire array, but some speculative conclusions will be drawn based on research on ordered micro-LEDs performed by H. W. Choi *et al.* from 2003 to 2006^{64,65,66,67,68,69,70,71}. Several plots from these papers will be carefully discussed, and the enhanced performance compare to broad-area LEDs can be concluded.

Nowadays in industry, the most common characterization of LED is the injected current vs. forwarded voltage (I-V curve) and the brightness or the output power vs. the injected

current (L-I curve). The inspection of the I-V curve gives the threshold voltage, and the L-I curve indicates the efficiency of conversion from electricity to light, both of which address how efficient of the light emission. To attain good I-V or L-I characteristics, the improvement of the ohmic contact is needed, but this is still under research.

4.2.1. Improved Current Spreading, Heat Dissipation and Emission Uniformity

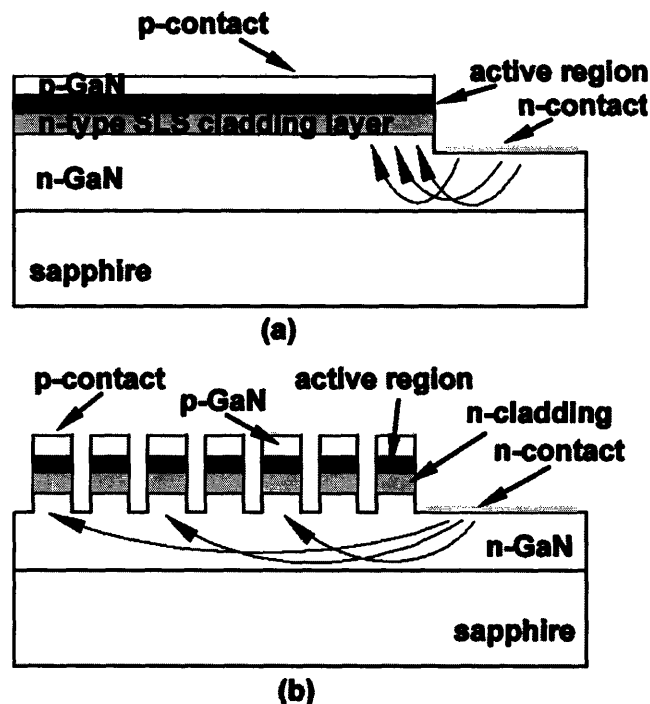


Figure 27⁶⁹: Schematic diagram illustrating current flow (and current crowding effects) in (a) broad-area LED and (b) micro-ring LED.

Figure 27 shows a side-view sketch of a micro-LED structure consisting of (from bottom to top): an n-doped GaN buffer layer, an n-doped AlGaIn/GaN strained-layer-superlattices (SLS), a multi- quantum well active region of InGaIn/AlGaIn,

a p-doped AlGaIn/GaN SLS, and a Mg-doped p-GaN layer. The micro- elements force the current to flow horizontally along the broad-area n-type GaN buffer layer which gives rise to better current spreading due to a lower lateral resistivity compared to the perpendicular resistivity due to the parallel vertical conduction along the micro- elements axes through the n-doped SLS layers. This leads to much more uniform light emission across the whole area than in the broad-area LED. Also, the improved current spreading leads to better heat dissipation.

4.2.2. Comparable I-V Characterization and Much Higher Power Saturation

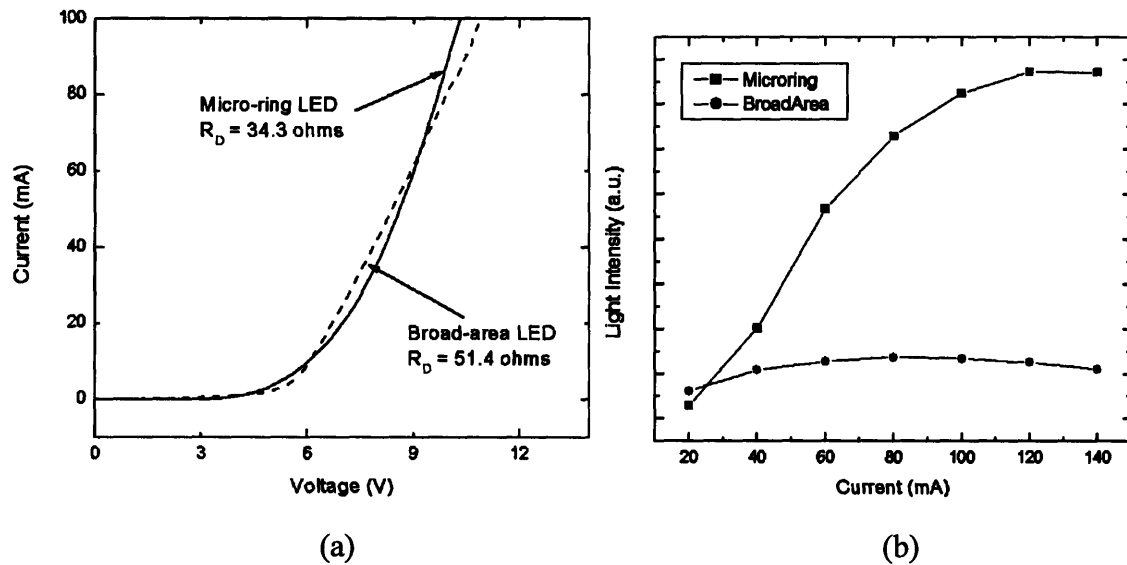


Figure 28⁶⁹: (a) I-V plots for the UV broad-area and micro-ring LEDs; (b) L-I plot of light output power as a function of current for the broad-area and micro-ring LEDs.

In Figure 28a, there are two regimes. At lower injection levels (current < 40 mA), the micro-ring LED has inferior characteristics, turning on at 6.94 V (compared to 5.83 V for

the broad-area LED), with a leakage current (at $V = -3$ V) of 70.48 mA (compared to 0.75 mA for the broad-area LED). In contrast, at high injection level, the micro-ring LED has a lower differential series resistance of 34.3 Ω (compared to 51.4 Ω for the broad-area LED).

In the low injection current regime, the micro-ring LED is operating at a higher current density due to the smaller junction area of the interconnected network. The higher turn-on voltage results from the current injection through the micro-scale contact and less total contact-area, with a higher contact resistance. The higher current density accounts partially for the higher leakage current. In the high injection current regime, the reduced differential series resistance results from the improved current spreading.

Figure 28b shows a plot of light intensity vs. current for equivalent light-emission area (the junction area) for a micro-ring LED vs. a broad-area LED. Reading from the figure, the output power saturates at 80 mA for the broad-area LED and 120 mA for the micro-ring LED. The micro-ring LED emits 3 times more optical power at this current 120 mA compared to the broad-area LED. The higher optical output power can be expected from the more uniform light emission across the chip, and the increase in saturation current can be explained by the reduced differential series resistance (thus reduced current crowding) and a *heat sinking effect*.

4.3.3. Enhanced Extraction Efficiency of Micro-LEDs

There are two additional factors accounting for the effects discussed above: reduced re-absorption and enhanced sidewall extraction.

Re-absorption in the chip material itself is a big obstacle for efficient light extraction in broad-area LEDs, and this is why the micro-LED idea initially came forward. With micro-LEDs, the likelihood of generated photons being emitted from the device before re-absorption is increased. Taking GaN as discussed above as an example, the absorption coefficient at 470 nm is reported to be approximately 10^3 cm^{-1} , corresponding to an absorption length $\sim 10 \text{ }\mu\text{m}$ ⁶⁴. Accordingly, lower absorption is expected in micro-GaN LEDs, because of the much higher chance that photons will reach the surfaces without being absorbed, and then be extracted out, particularly for micro-LEDs with radii of less than 10 μm .

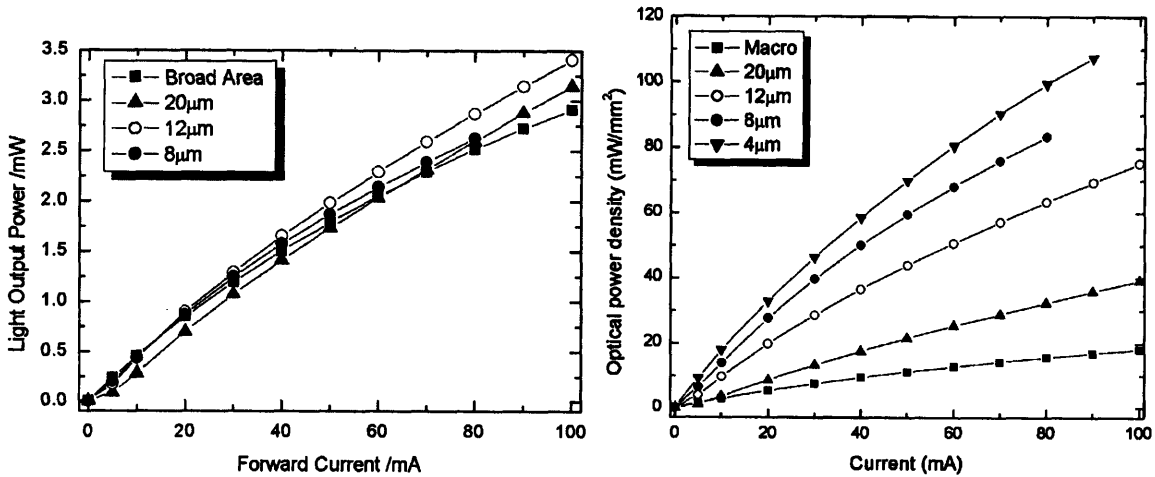
It is more responsible to conclude that the extraction efficiency, rather than the internal quantum efficiency, is responsible for the improvement of the external quantum efficiency. The sidewalls of micro-disk or micro-ring LEDs can facilitate the light extraction because the photons reaching the sidewall without suffering absorption are scattering off the sidewalls so that more photons get escaped⁶⁶.

Noting that for a pillar array (or even a nanowire array) LED the output light with no coherent phase or direction can be extracted either through the sidewalls or along the vertical axial direction, there is a certain emitting cone from which the light can be collected from the top. While for a LD, there is only the light coming out from the axial direction, and no such benefit to the extraction efficiency from the sidewall effect would be expected for applications to LDs.

4.2.4. Increasing Output Power Density with Decreasing Diameters

Elemental diameter (μm)	Chip area (μm^2)	Number of elements	Total active area (μm^2)	Turn-on voltage (Volts)	Operation voltage @20mA
8	240000	625 (25x25)	31416	7.62	7.48
12	240000	400 (20x20)	45239	4.64	4.60
20	240000	256 (16x16)	80425	3.12	3.49
Broad Area	240000	1	160000	3.42	3.80

(a)



(b)

(c)

Figure 29: (a)⁶⁴ Summary table of different tested LEDs; (b)⁶⁴ Light output–current (L–I) plots of micro-LEDs with different diameters; (c)⁶⁵ Active-area-normalized optical power output vs. current characteristics of micro-LEDs.

With the same device area (chip area) 240000 um^2 , the effective emission area ratio (the filling factor = active light-emission area/ chip area) for micro-disk LEDs with the diameter of 8 um, 12 um, 20 um and the broad-area LED is calculated to be 13.09%, 18.85%, 33.51% and 66.67%, respectively, according to the summary table in Figure 29a. However, the total amount of output light is more or less the same for both micro-LEDs with various sizes and a broad-area LED, which indicates a comparable output power with the same chip size. The plots of the normalized optical power density in units of miliwatt per unit active area give strong evidence of enhanced light-emitting capability for smaller-sized LEDs. The photograph below gives a good example showing the more uniform and non-degrading light emission for a micro-LED compared to a broad-area LED with the same chip area.

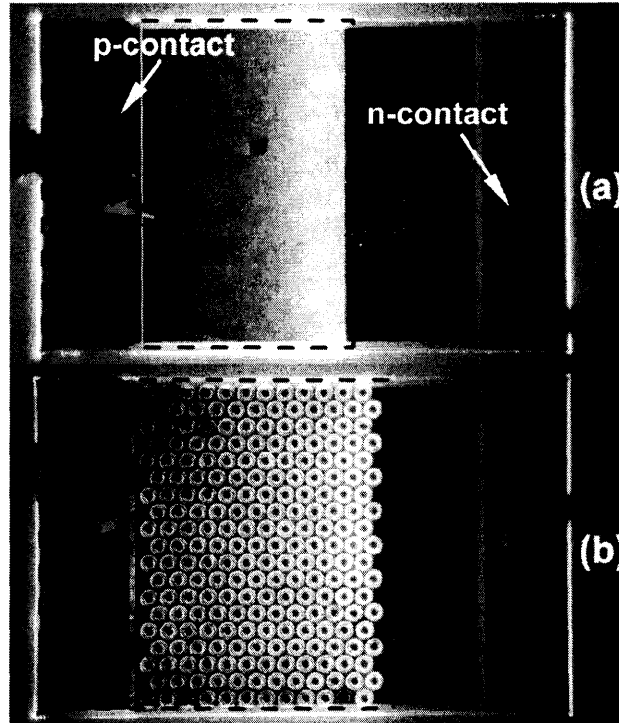


Figure 30⁶⁹: (Color online) Microphotograph of the (a) broad-area UV LED and (b) micro-ring LED operated at 50 mA. The current spreading metal regions are highlighted in dotted lines.

4.2.5. Shape-Dependent Optoelectronic Properties

(i). Micro-ring vs. micro-disk

High surface-area (top plus sidewall) to light-emission-area (top) ratio accounts for high light-extraction (photon escape) through the sidewalls^{65,66}. In this experiment leading to Figure 31, LEDs had identical total light-emission areas (top surface) of $120 \times 400 \mu\text{m}^2$, but with diameters for micro-disks and micro-rings of 20 μm and 12 μm (inner)/20 μm (outer). The higher output power density of micro-ring LED compared to that of the micro-disk LED is the result of further enhanced sidewall scattering, due to the even

larger sidewall-surface area to light-emission area ratio for micro-ring LEDs⁶⁶.

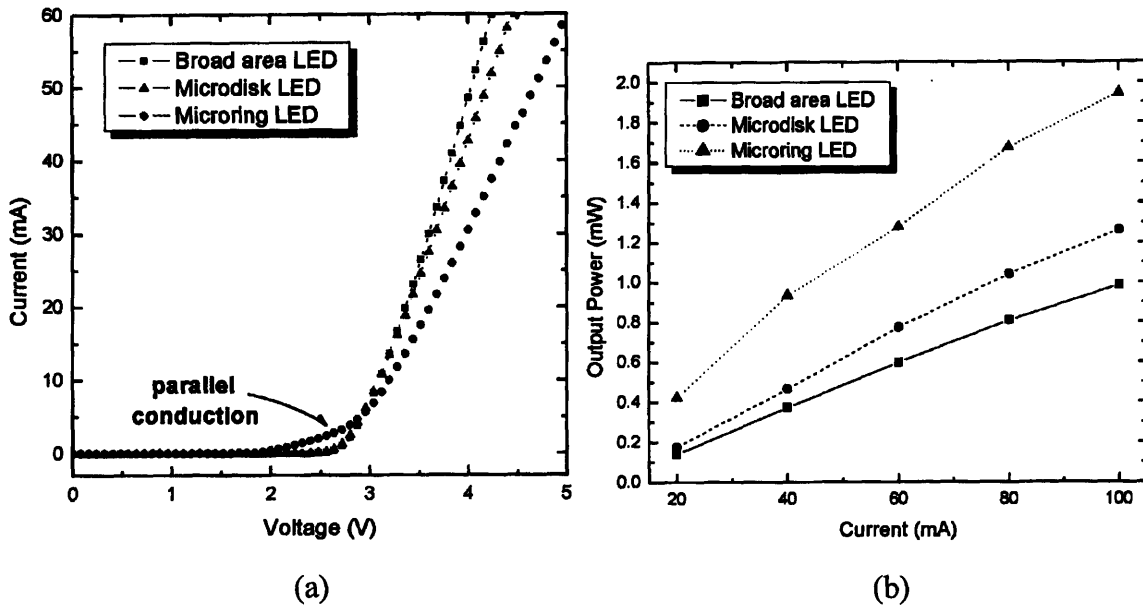


Figure 31⁶⁶: (a) I-V and (b) light-emission-area-normalized L-I curves of the micro-ring, micro-disk and broad-area LEDs.

(ii). Hexagonal vs. micro-disk

Figure 32 shows results for micro-disk LEDs and hexagonal-closed-packed honeycomb micro-LEDs (“hex-LED”) with 50 μm unit diameters and 25 μm side lengths. Having a higher filling factor on the same chip area (78% compared to 63%)⁷¹, the hex-LED has a larger light emission area than the micro-disk LED. At 50 mA, the micro-disk LED emits 50% more light than a broad-area LED. With the hex-LED, an additional 50% increase in the output power is observed, twice as efficient as a comparable broad-area LED, assuming equal light-emission area (active area). The authors of this paper claimed that *filling factors* as high as 95% could be achieved by further reducing the separation distance with conventional photolithographic techniques.

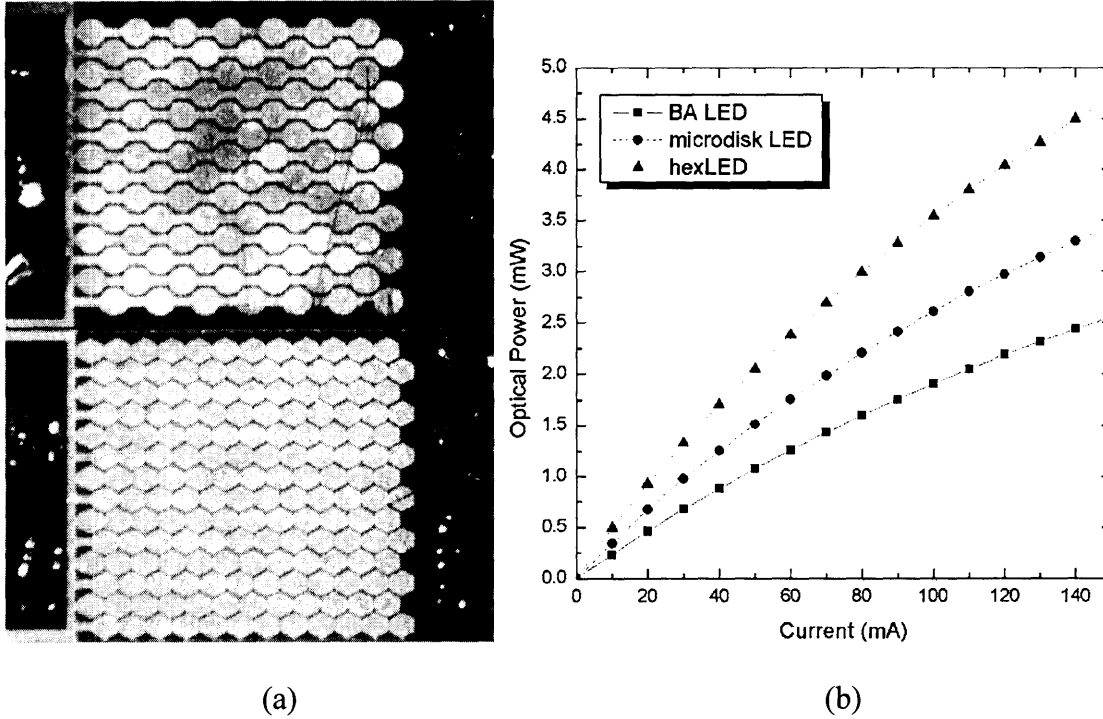


Figure 32: (a)⁷⁰ Microphotograph of a micro-disk LED (top) and a hex-LED (bottom) driven at 5 mA; (b)⁷¹ L-I curves of a hex-LED, a micro-disk LED and a broad-area LED, normalized to the same light-emission area

4.3. Chapter Summary

While the extraction efficiency is improved for nanowire-array LEDs, because nanowires have high surface wall area to junction area ratios, the effects of surface states are expected to degrade the internal quantum efficiency of nanowire-array LEDs compared to broad-area LEDs. However, the degradation of the internal efficiency can be significantly reduced through the use of epitaxial cladding or passivation layers. Also, the radiative recombination can be enhanced by the reduction of the piezoelectric field due to the strain relaxation in nanowires. The net effect on the internal quantum

efficiency, or further extended to the external quantum efficiency, cannot be simply concluded in this thesis.

Chapter 5 Intellectual Property (IP) Analysis

5.1. Overall View of IP Environment

To find out whether this proposed design will run into the IP infringement, different keywords have been tried in the searching engine at www.uspto.gov. There are hundreds of patents and published applications associated with semiconductor heterostructure nanowires, many of which held by the two companies Nanosys and NICHIA. But as predicted, there is only one patent related to the application of this kind of nanowire array as LD, and less than 5 as LED, because the nano-light-emitting device is still a very new area around the world.

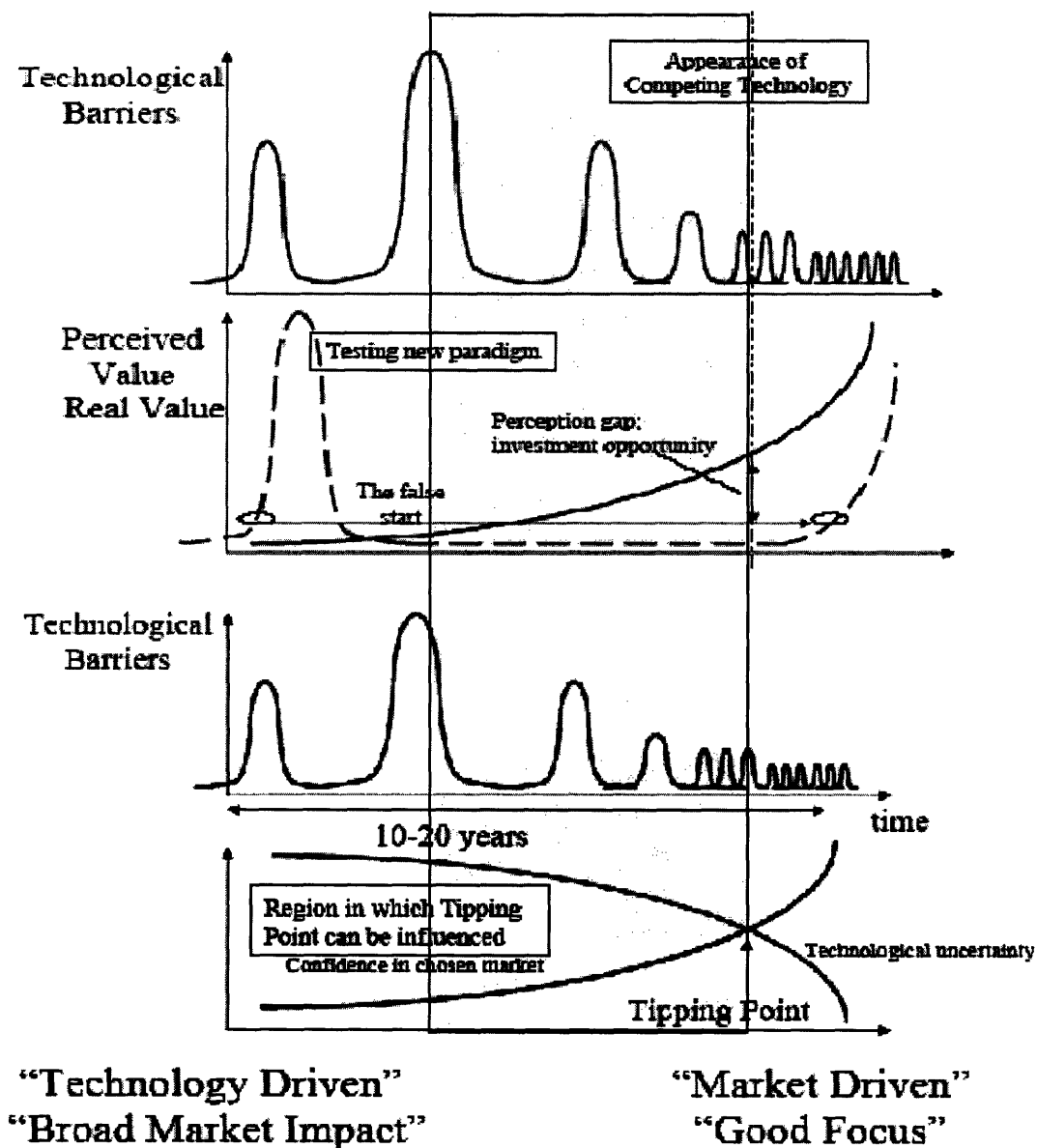


Figure 33⁷²: Technological barriers diagrams.

According to the technological barrier diagrams, the technology of the templated arrays of heterostructural semiconductor nanowires is right in the middle gap regime (the yellow shaded region), which means it already surpassed the largest barrier, but it still has to face several small barriers as well as rising competitors. So it is a very good time

to patent as best as possible right now. It is better to invest in a Fab at the biggest perception gap, but not at this moment.

5.2. Specific Example of Relevant IP

Two most important relevant IP files were studied to compare with the proposed structure and technology.

5.2.1. Laser: Patent US 6996147⁸

This issued patent of an LD covers lots of applications, which will be a big hurdle to the patent application of the thesis-proposed structure or device. Although they didn't make any of the potential applications or devices realized, there would be much trouble if not careful enough.

The sketched laser design made from nanowire array is similar to the thesis-proposed one (Figure 34), however, no specific information is given, such as the composition of materials and the dimensions of the structures. In spite the wide range this patent covers, the newly developed idea in the thesis-proposed design of inserting the graded buffer layer into the nanowire and the substrate, and making use of Si wafers to grow optoelectronic structures is able to avoid the IP conflict.

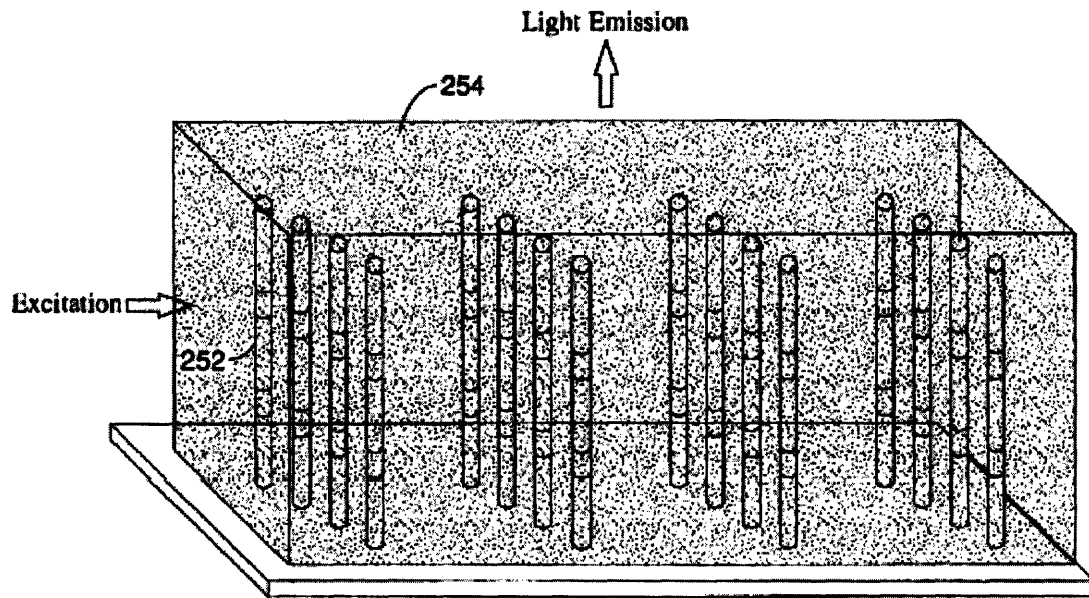


Figure 34⁸: Schematic drawing of the light emission from the heterostructural nanowire array.

5.2.2. LED: Patent Application Publication US 2005/0194598⁶⁰

The high-brightness LED is invented by K-M Kim *et al.* The nanorod-array structure is shown in Figure 35. However, while the figure indicates an ordered array, the publication text does not. This patent application publication exhibits good optical properties as an LED (Figure 36).

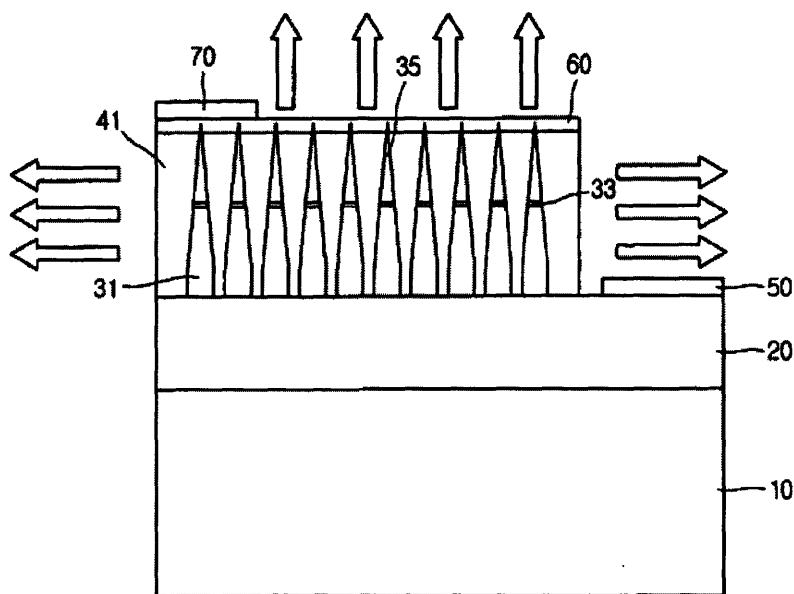


Figure 35⁶⁰: The schematic diagram of a structure of the invention consisting of an InGaN/GaN nanowire array for light emitting. No. 41 indicates the transparent insulating material covering the ordered nanowire array.

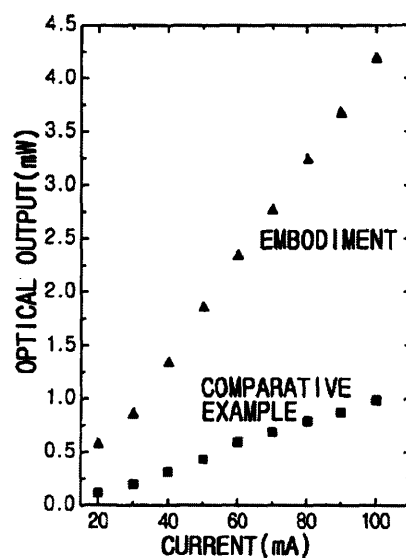


Figure 36⁶⁰: L-I curves of the invented LED and its conventional counterpart.

The weakness of this invention is the substrate this patent claimed to use. As they are using GaN-sapphire wafers, which would be much more expensive and more difficult to

be integrated into existing electronic devices compared to the design of growth from Si substrate.

5.3. Chapter Summary

The study of associated intellectual properties reveals that there is plenty of space ahead for the thesis-proposed structure and/or the light emitting device to apply for the patents. Inspiring many weaknesses of the issued patents, we still need to be careful to avoid the impingement, because those few issued patents claimed to cover a lot of areas.

Chapter 6 Market Analysis and Business Model

Applications of the proposed light-emitting device extend far beyond the traditional usages of LDs and LEDs. The potential for success in the rapidly growing high brightness LED and LD markets is tremendous as U.S. sales of lighting products totaled to \$11.9 billion for 2005⁷³ with a significant and increasing portion of that figure coming from solid state lighting sources. In addition to solid state lighting, there are new applications which could potentially utilize a device such as this and open new markets in the Si world for nanowire based light emitters.

6.1. Market Analysis

6.1.1. LED Market

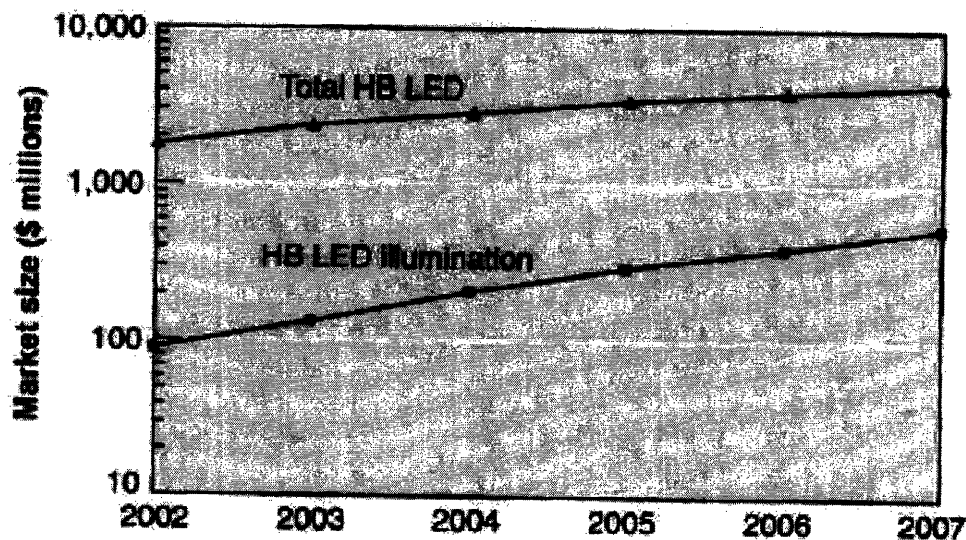


Figure 37⁷³: The predicted market size of high-brightness (HB) LED and HB LED illumination.

Projections made by *Laser Focus World* in 2002, Figure 35, indicate that illumination applications will account for 12% of the high-brightness LED market in 2007 compared to just 5% today. The entire HB LED market will grow from \$3.9 billion this year to \$4.4 billion in 2007 according to their model.

However, other than this old forecast, a new prediction brought forward by Dr. Alan Mills suggests⁷⁴:

“Even with little penetration of the general lighting market, high-brightness LED sales for 2005 is \$4-5 billion, with 15–20% growth anticipated for 2006. The market is expected to be \$7-8 billion by 2008, then up to \$11 billion by 2010--- mainly a result of the complete superiority of LEDs for most colored lighting requirements and the success of white LED backlighting for mobile devices”.

6.1.2. LD Market

The average annual growth rate (AAGR) of world laser diode market from 1997 to 2005 was approximately 8.1% per year according to Figure 36 and the sales revenue was \$3.23 billion in 2005 compared to \$3.20 billion in 2004. Laser diodes continue to represent

59% of total commercial laser revenues, which indicates that the decrease in average selling price has been offset by an increase in shipments of laser diodes.

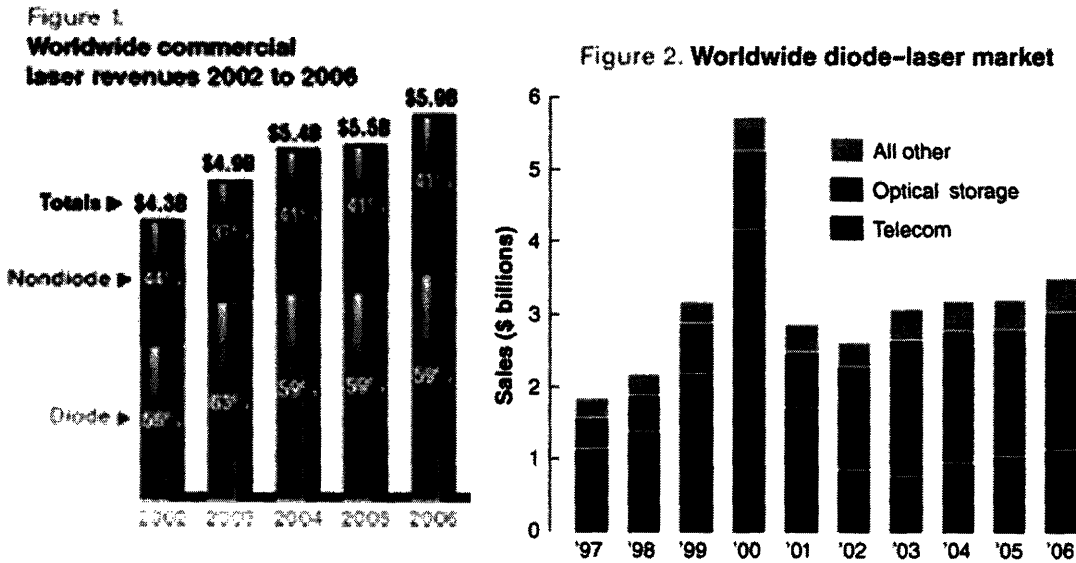


Figure 38⁷³: Data of the laser and laser diode market.

The history of the laser diode market shows the continuing recovery since the peak of the telecom bubble around 2000. All segments are forecast to grow in a relatively narrow range, from 7.8% to 9.3% in the near future, while overall, the laser diode market is forecasted to grow appreciably at 9% to \$3.52 billion in 2006. Combining the LED and LD segments, it will be a huge light-emitting market to dive in.

6.2. Constrains of Investment on the Technology: Funding and Big Players (Competitors)

6.2.1. Funding

Despite slowing growth of public spending, governments worldwide are spending some \$4 billion per year, Figure 39, on nanotechnology projects⁷⁵. With the addition of corporate and private investments, this could bring the total spending level to as much as \$8 billion per year. Policy makers, universities, and professional organizations have clearly recognized the value and also the complexity of merging disciplines in order to exploit new developments in nanotechnology.

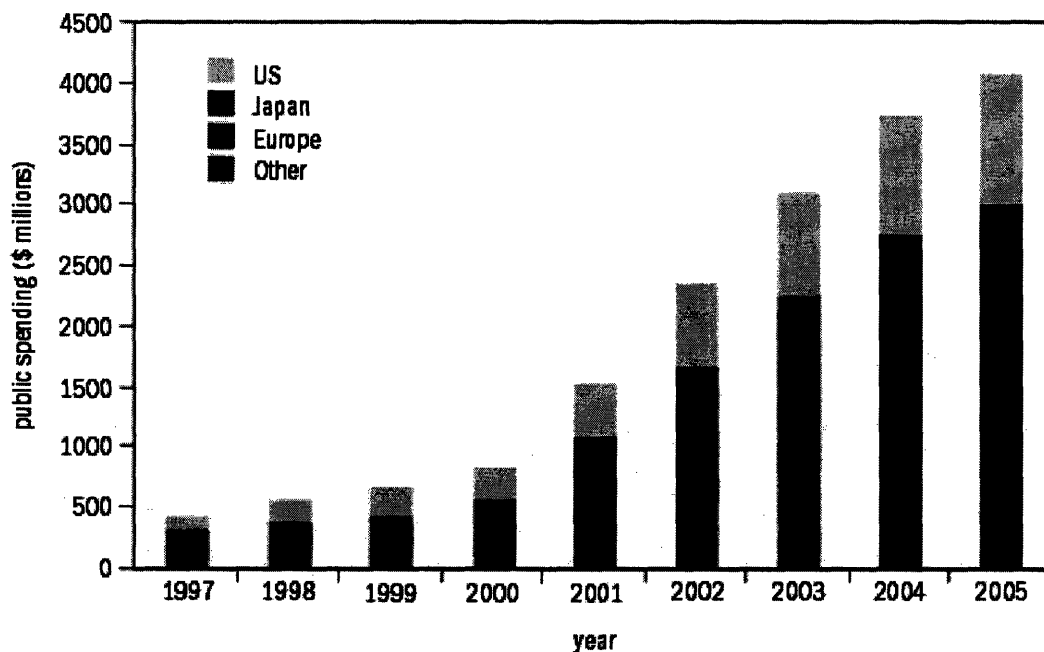


Figure 39: Worldwide government spending on nanotechnology programs [NSF and Strategies Unlimited, 2005].

6.2.2. Competition

Tom Hausken, Optical Communication Components Practice Director at Strategies Unlimited, suggests “There is only business for a few **key suppliers**, plus some additional niche players”⁷⁶ in the laser diode manufacturing market. Despite slow sales climbing, the number of suppliers has expanded far beyond any reasonable value, to over 100⁷⁵. This is clearly excessive, even for this diverse market, and even allowing for a healthy number of start-up companies as candidates for acquisition. So far, there have been only a few consolidations and closures in this market segment. The virtual certainty of consolidation creates a strong demand for valuable intellectual property, especially if the technology is vastly superior to its alternatives.

6.3. Business Model (IP Model)

A comprehensive analysis of the advantages of a nanowire based light-emitting device has been explored in chapters three, four and five. Consistent with Figure 33, features of the device such as low cost, high reliability and great performance combined with the relative immaturity of nanotechnology suggest an IP business model the most attractive type of start up company leverage this technology.

A new company having a new technology, supported by VC, can do great business,

especially for a short-term objective, but licensing to key suppliers and sharing existing market is key to the company's survival as indicated in Figure 38.

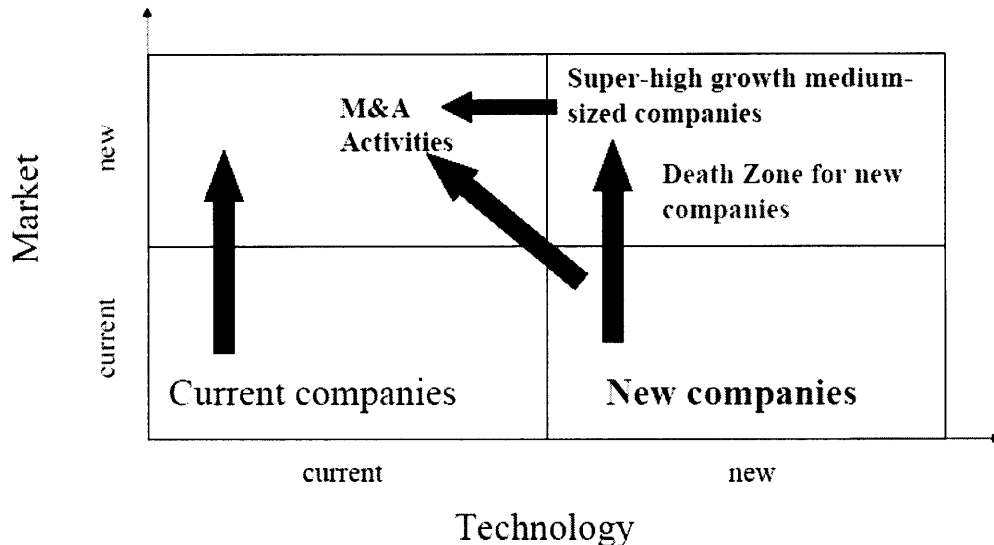


Figure 40⁷²: Illustration of Death Zone for new companies.

A nanowire based light emitting device has two strong arguments against investing in a new fab and instead licensing to big Si fabs (IP Model). First, GaAs LEDs or LDs working in the IR (infrared) range are very popular for the remote control or long distance transmission. The invisible communications enabled by a GaAs IR diode may lead to on-chip or chip-to-chip communications where all electronic and optoelectronic elements can be integrated together on a single chip, something highly advantageous to the Si logic world.

Second, if a nanowire LED array is used simply for lighting applications, the ability to grow the arrays on the cheapest Si wafers can help to cut down the cost of raw materials

compared to building diodes on highly expensive compound semiconductor wafers. Furthermore, for an existing Si fab there is no investment requirement to purchase new equipment making it very attractive for well-established semiconductor manufacturing corporations.

6.4. Chapter Summary

Clearly the most attractive proposal for a start up a company using this device concept is the based on an IP model. Applying for patents and then licensing them to key players in the semiconductor industry has enormous potential to take advantage of this technology. Combining the solid state lighting market of LEDs (\$3.9bn) and LDs (\$3.52 bn) estimates the industry revenue at \$7.42 billion for 2006. Next, assuming reasonable market share of a big semiconductor manufacturer as 20% and the royalty fee as 1.5% for profit, a simple calculation of IP model gives rise to the revenue of \$22.26 million. This figure should be enough to cover patent fees and repay initial investment funds.

Chapter 7 Conclusion

The complexity and promise of templated arrays of heterostructural semiconductor nanowires has prompted a detailed evaluation of both the device's technology and the device's market potential which are required to support a business model for a start-up. The proposed device has extraordinary characteristics such as highly improved reliability, improved extraction efficiency and non-significantly-degraded internal quantum efficiency, which will enable it to compete with other light emitting structures.

At the first sight, there seems to be a trade-off between the reliability and the performance achieved by this design. After careful examination, the reliability is improved by the reduction or even elimination of both the misfit dislocations and threading dislocations in nanowires. Whether or not the electrical and optical performance of the nanowire array will be improved must be explored by more research to make a concrete conclusion. The interplay of the three factors will ultimately contribute to the device's performance:

- 1) Enhanced extraction efficiency due to lower re-absorption and high sidewall effect.
- 2) Improved term of the internal quantum efficiency due to the strain relaxation only possible on the nano-scale.
- 3) Degraded internal quantum efficiency due to the high concentration of surface states.

Therefore, at this stage, the only thing can be concluded here is that the trade-off is not established, but it is tending to favor a win-win case for the relationship between the reliability and the performance of this device.

Further research on how the core diameter, the shell thickness and the periodic spacing between nanowires are going to affect the overall properties (reliability and performance) of the arrayed device must be done both experimentally and theoretically to achieve the optimal dimensions for device performance.

Regardless of the long term success of the device as a commercial product, it is clear that now is the right time to patent the proposed templated array of heterostructural semiconductor nanowires.

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